EN2042102 วงจรไฟฟ้าและอิเล็กทรอนิกส์
Circuits and Electronics

บทที่ 3 วิเคราะห์วงจรไฟฟ้า

สาขาวิชาวิศวกรรมคอมพิวเตอร์

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CURRENT SOURCES

❖ In previous chapters, the voltage source was the only source appearing in the circuit analysis.

❖ This was primarily because voltage sources such as the battery and supply are the most common in our daily lives and in the laboratory environment.

❖ We now turn our attention to a second type of source, called the **current source**.
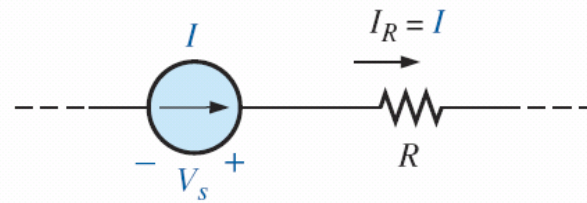
CURRENT SOURCES

❖ Although current sources are available as laboratory supplies, they appear extensively in the modeling of electronic devices such as the transistor.

❖ Their characteristics and their impact on the currents and voltages of a network must therefore be clearly understood if electronic systems are to be properly investigated.
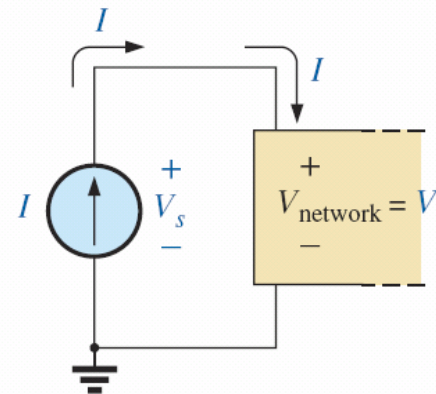
LOGO

CURRENT SOURCES

❖ The current source is often described as the *dual* of the voltage source.

❖ Just as a battery provides a fixed voltage to a network, a current source establishes a fixed current in the branch where it is located.

(a)

(b)

FIG. 8.1 *Introducing the current source symbol.*

CURRENT SOURCES

❖ In general, *a current source determines the direction and magnitude of the current in the branch where it is located.*

❖ Furthermore, *the magnitude and the polarity of the voltage across a current source are each a function of the network to which the voltage is applied.*

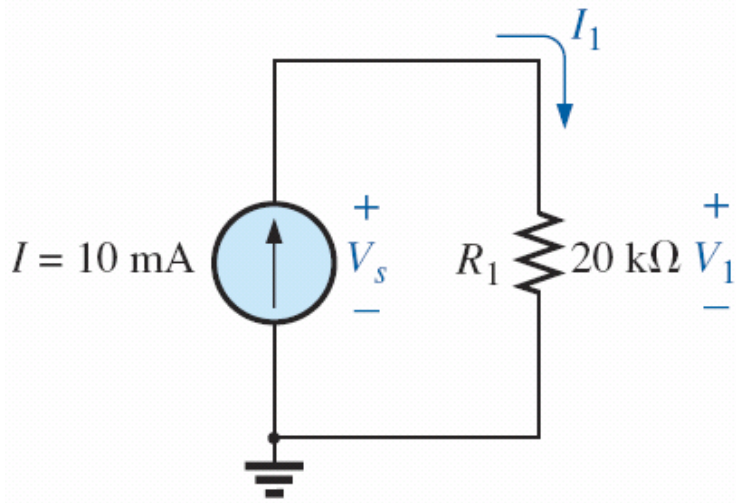**FIG. 8.2** *Circuit for Example 8.1.*

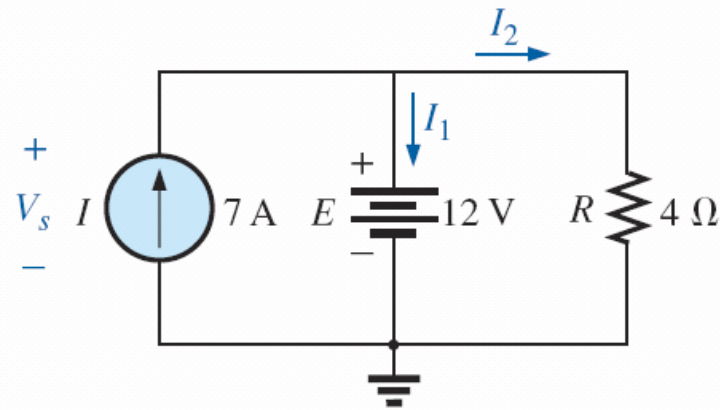**FIG. 8.3** *Network for Example 8.2.*
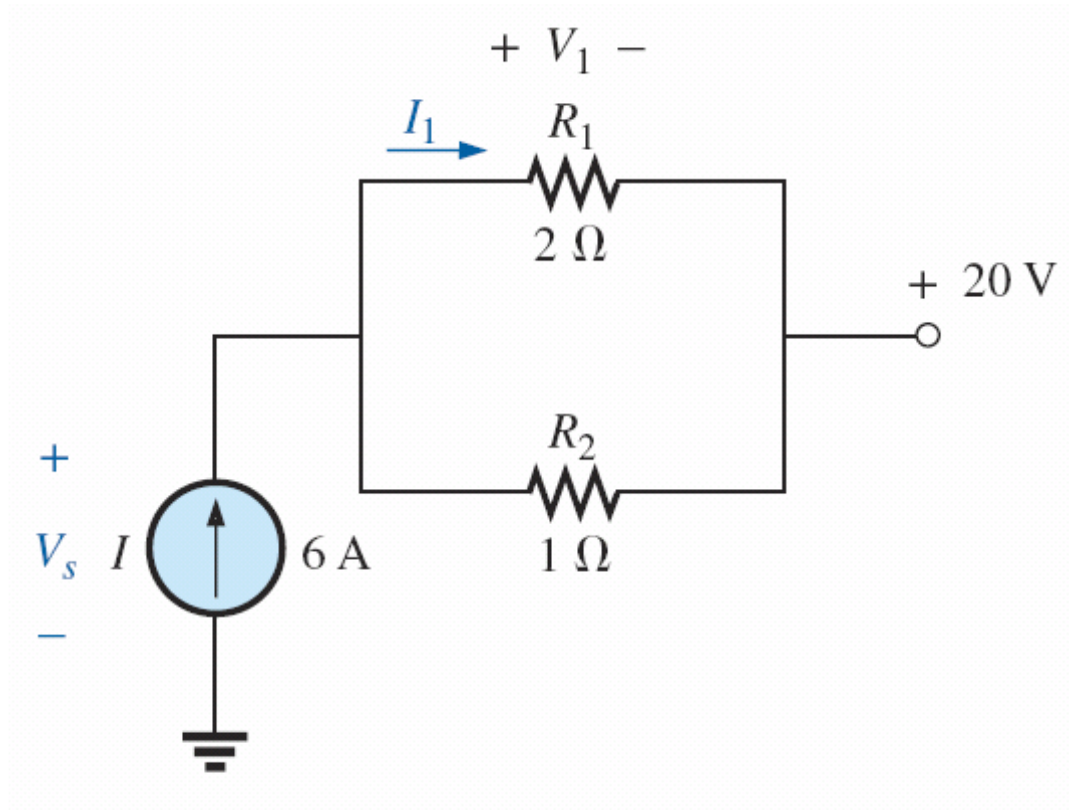
FIG. 8.4 *Example 8.3.*

SOURCE CONVERSIONS

❖ The current source appearing in the previous section is called an *ideal source* due to the absence of any internal resistance.

❖ In reality, all sources—whether they are voltage sources or current sources—have some internal resistance in the relative positions shown in Fig. 8.5.
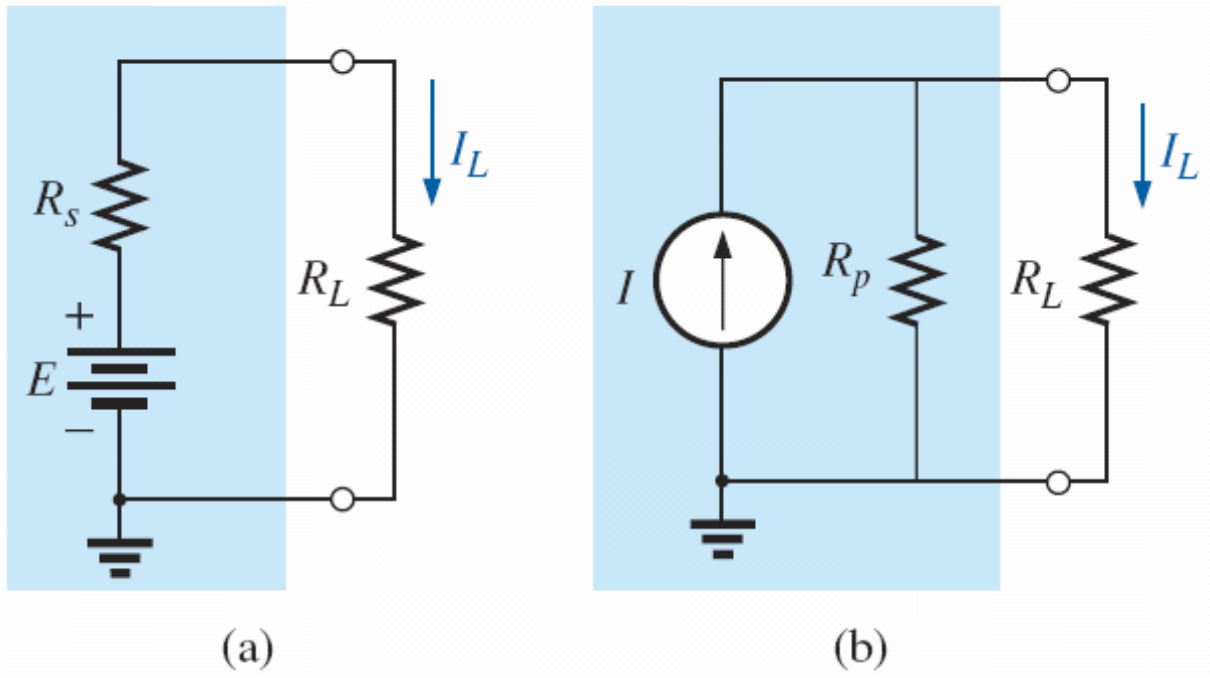
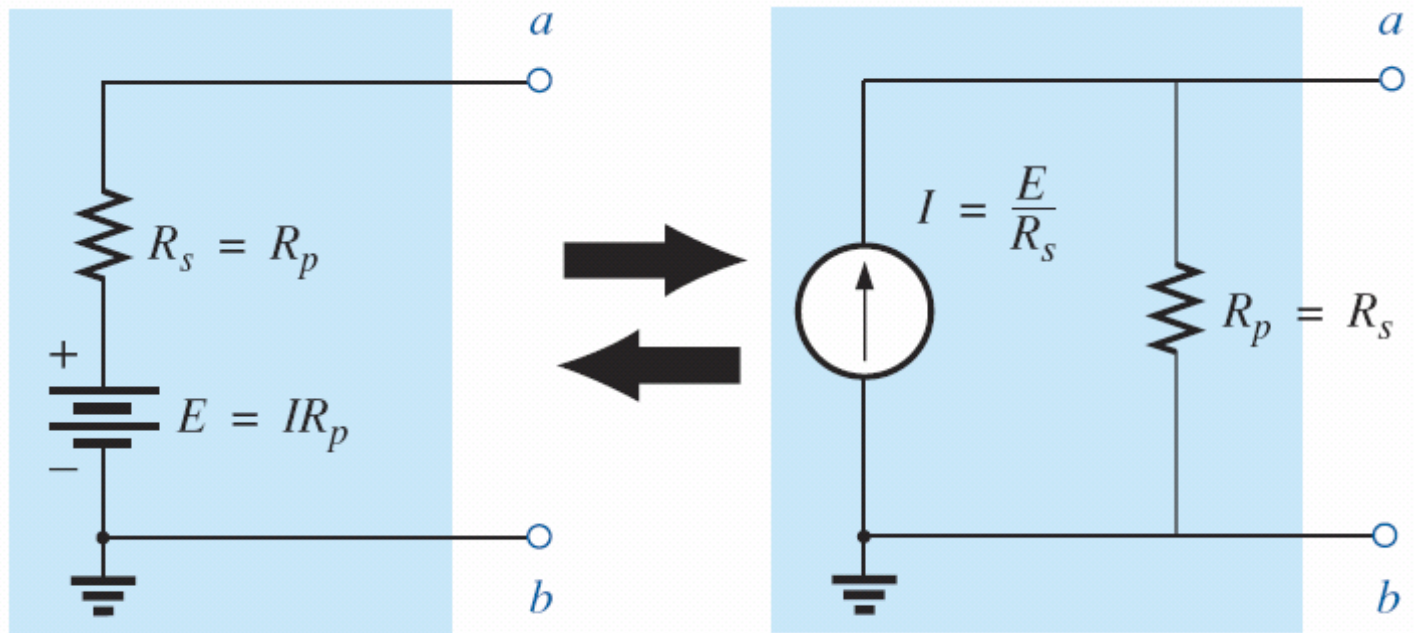**FIG. 8.5** *Practical sources: (a) voltage; (b) current.*

SOURCE CONVERSIONS

FIG. 8.6 *Source conversion.*

SOURCE CONVERSIONS

❖ It is important to realize, that *the equivalence between a current source and a voltage source exists only at their external terminals.*
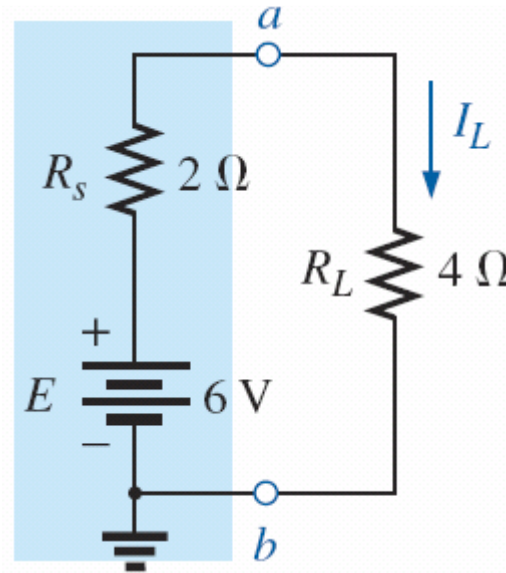

FIG. 8.7 *Practical voltage source and load for Example 8.4.*
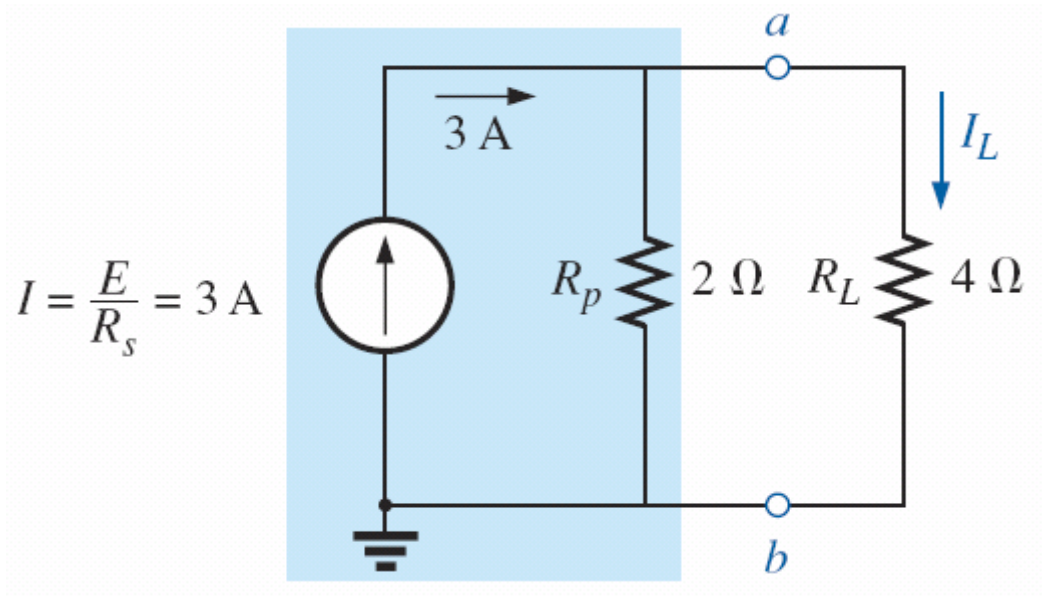
SOURCE CONVERSIONS

FIG. 8.8 *Equivalent current source and load for the voltage source in Fig. 8.7.*
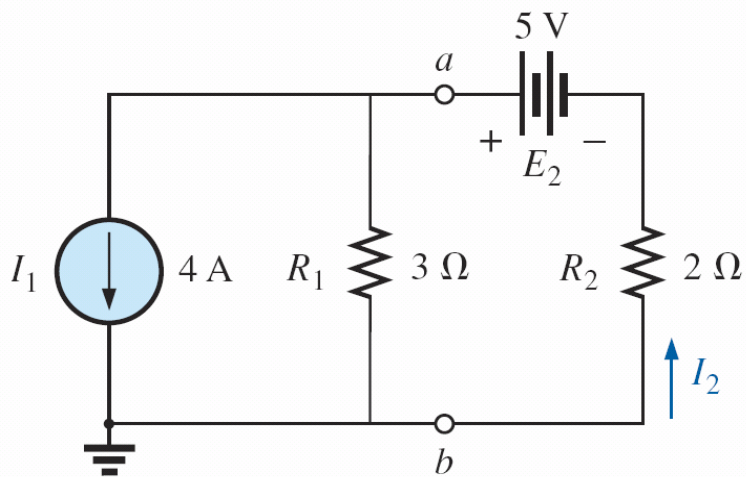
SOURCE CONVERSIONS

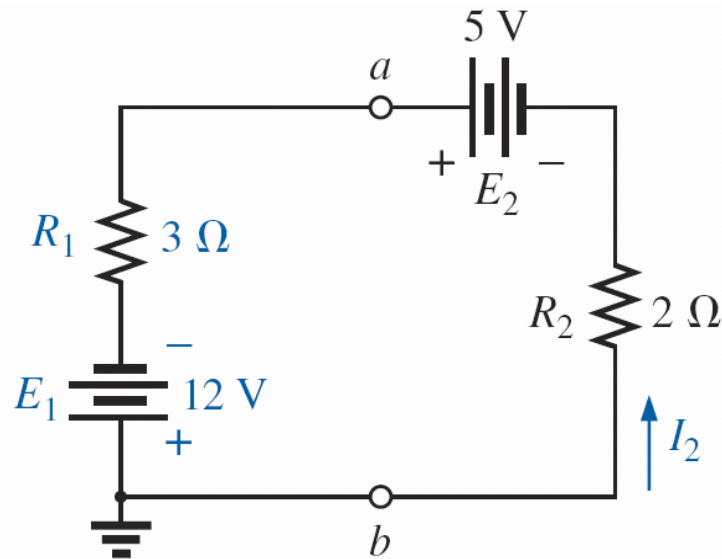**FIG. 8.9** *Two-source network for Example 8.5.*

FIG. 8.10 *Network in Fig. 8.9 following the conversion of the current source to a voltage source.*

❖ We found that voltage sources of different terminal voltages cannot be placed in parallel because of a violation of Kirchhoff's voltage law.

■ Similarly, *current sources of different values cannot be placed in series due to a violation of Kirchhoff's current law.*

❖ However, current sources can be placed in parallel just as voltage sources can be placed in series.

- In general, *two or more current sources in parallel can be replaced by a single current source having a magnitude determined by the difference of the sum of the currents in one direction and the sum in the opposite direction. The new parallel internal resistance is the total resistance of the resulting parallel resistive elements.*
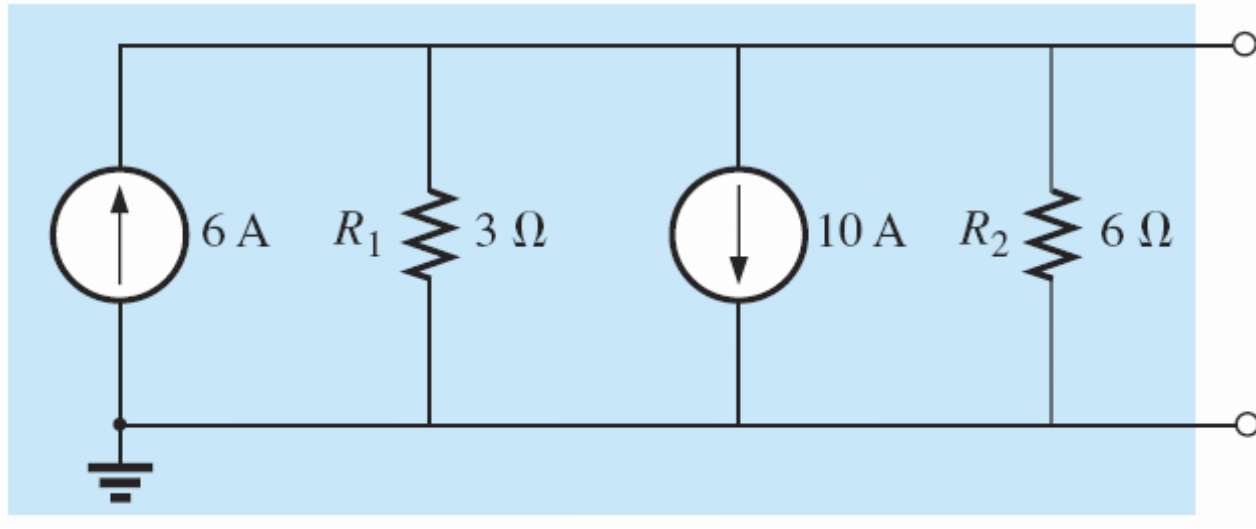
FIG. 8.11 *Parallel current sources for Example 8.6.*

CURRENT SOURCES IN PARALLEL

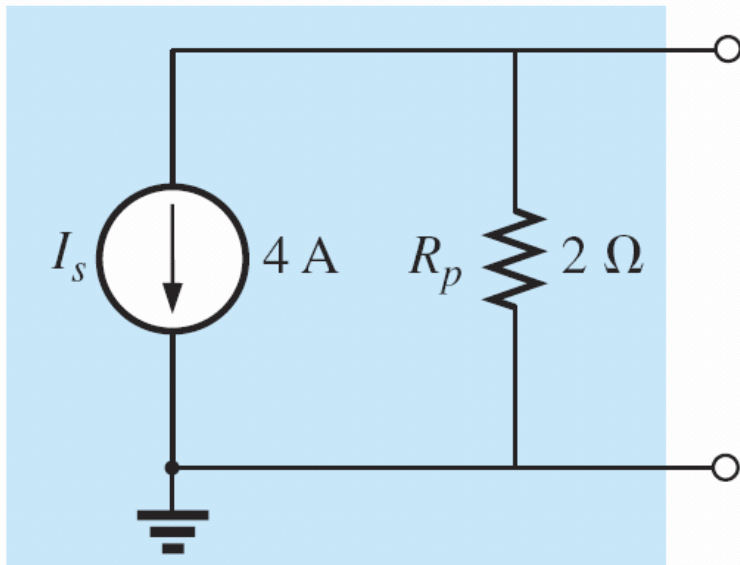

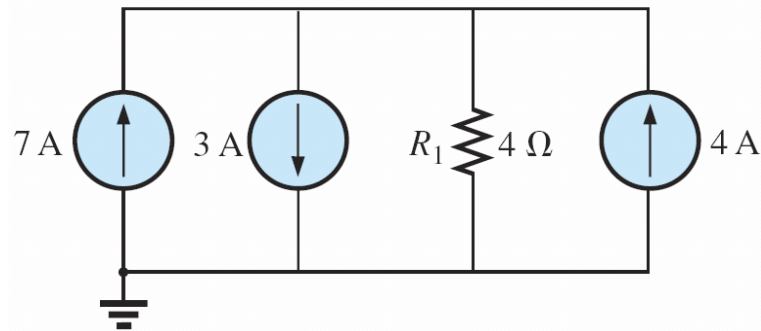FIG. 8.12 *Reduced equivalent for the configuration of Fig. 8.11.*
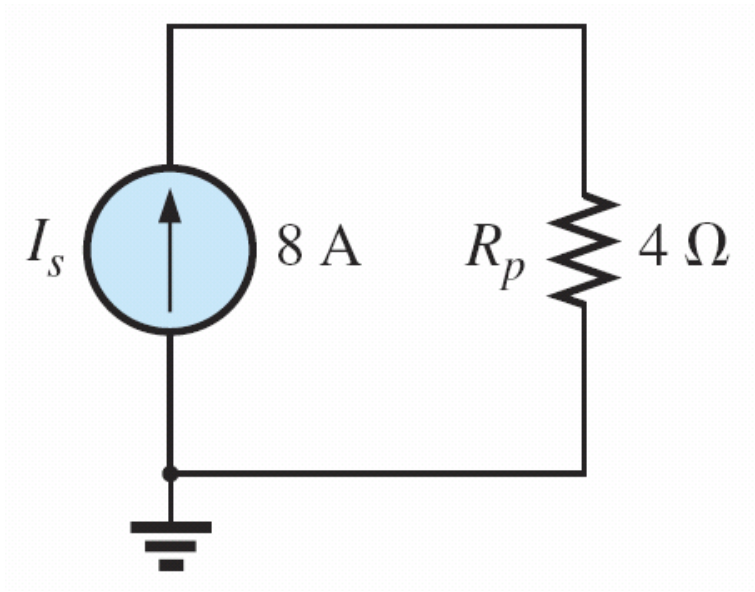

FIG. 8.13 *Parallel current sources for Example 8.7.*
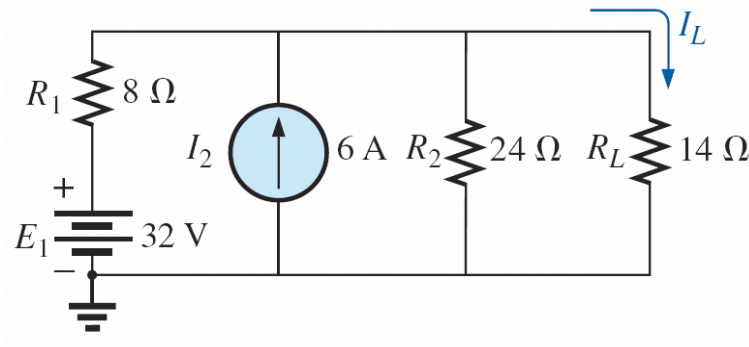
FIG. 8.14 *Reduced equivalent for Fig. 8.13.*

FIG. 8.15 *Example 8.8.*
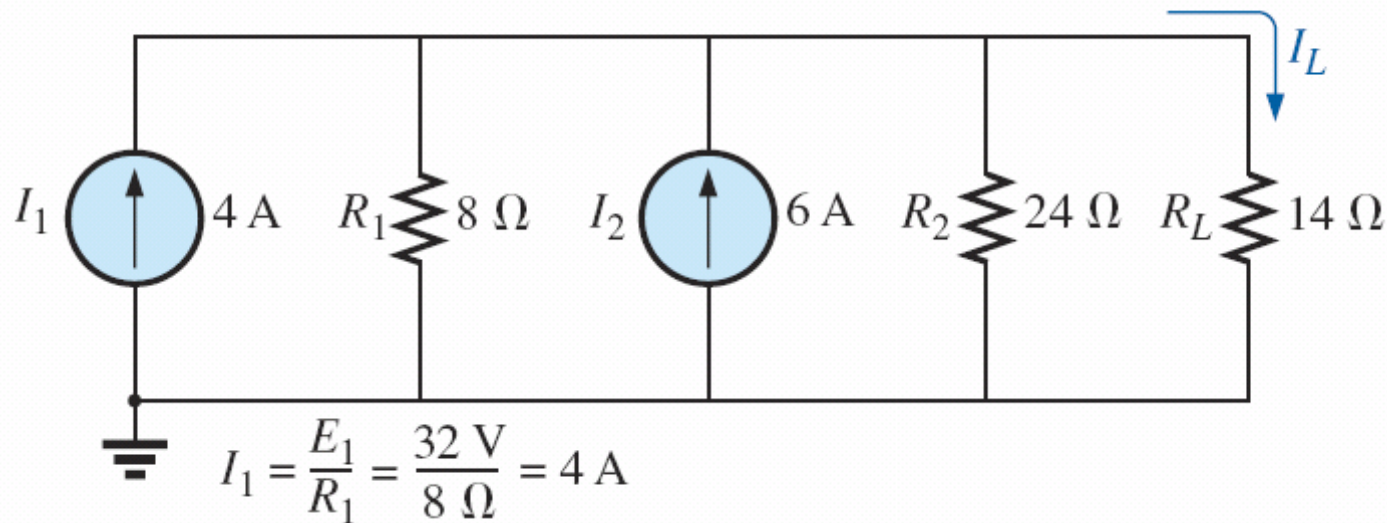
$$I_1 = \frac{E_1}{R_1} = \frac{32\ V}{8\ \Omega} = 4\ A$$

FIG. 8.16 *Network in Fig. 8.15 following the conversion of the voltage source to a current source.*
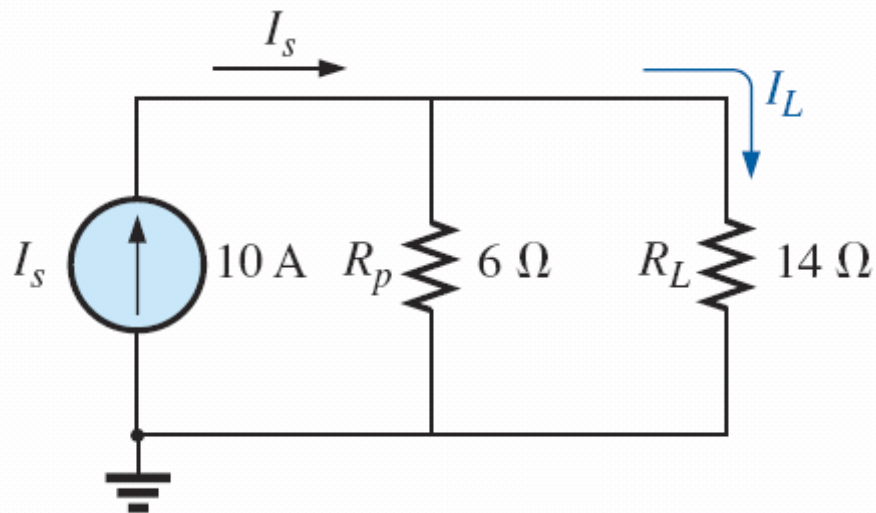
FIG. 8.17 *Network in Fig. 8.16 reduced to its simplest form.*

CURRENT SOURCES IN SERIES

❖ The current through any branch of a network can be only single-valued.

❖ For the situation indicated at point *a* in Fig. 8.18, we find by application of Kirchhoff's current law that the current leaving that point is greater than that entering—an impossible situation.

  ▪ Therefore, *current sources of different current ratings are not connected in series,* just as voltage sources of different voltage ratings are not connected in parallel.
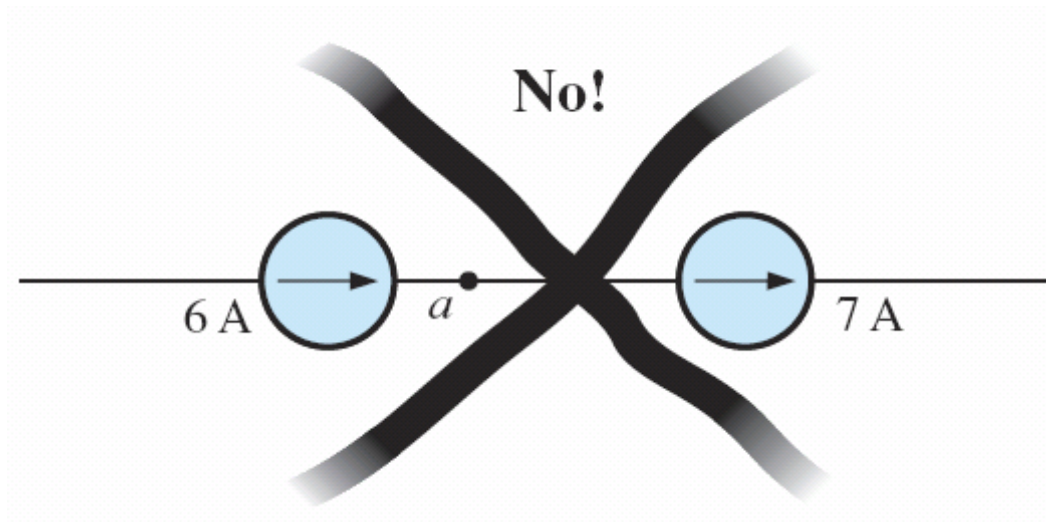
LOGO

CURRENT SOURCES IN SERIES
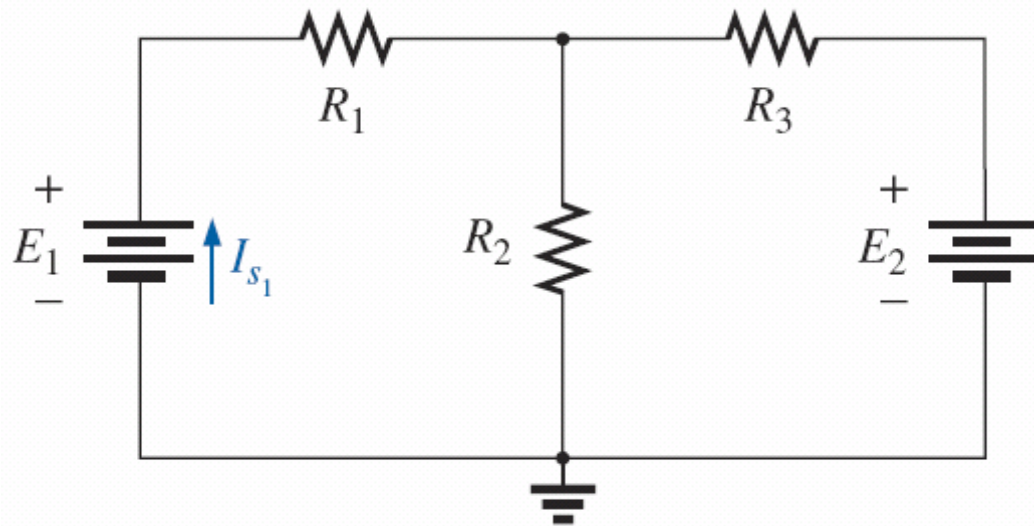

FIG. 8.18 *Invalid situation.*

FIG. 8.19 *Demonstrating the need for an approach such as branch-current analysis.*

BRANCH-CURRENT ANALYSIS

Branch-Current Analysis Procedure

1. *Assign a distinct current of arbitrary direction to each branch of the network.*

2. *Indicate the polarities for each resistor as determined by the assumed current direction.*

3. *Apply Kirchhoff's voltage law around each closed, independent loop of the network.*

BRANCH-CURRENT ANALYSIS
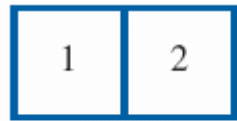
Branch-Current Analysis Procedure

4. *Apply Kirchhoff's current law at the minimum number of nodes that will include all the branch currents of the network.*

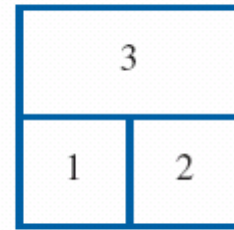5. *Solve the resulting simultaneous linear equations for assumed branch currents.*
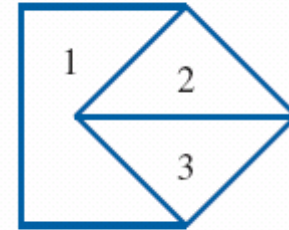
Branch-Current Analysis Procedure

FIG. 8.20 *Determining the number of independent closed loops.*

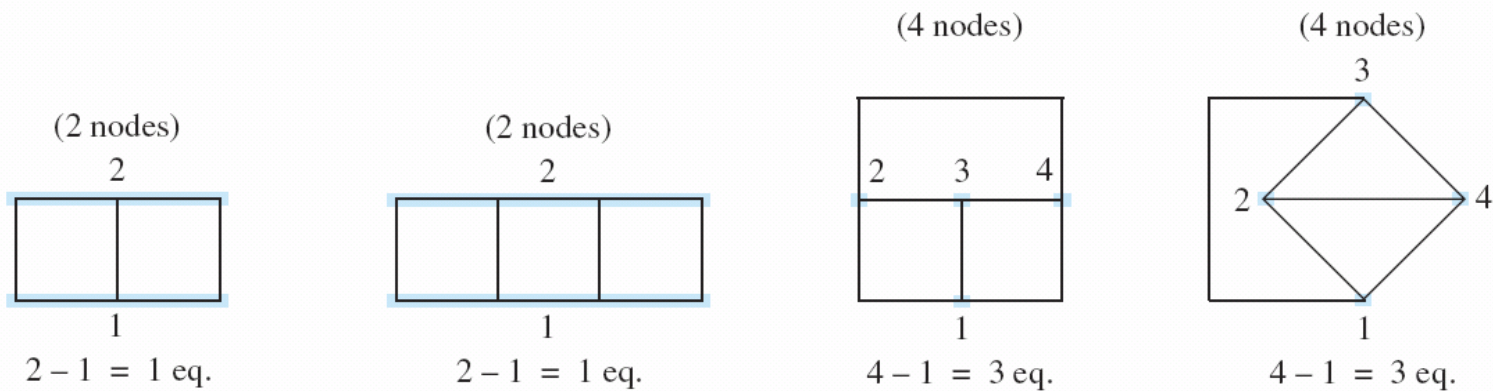**FIG. 8.21** *Determining the number of applications of Kirchhoff's current law required.*
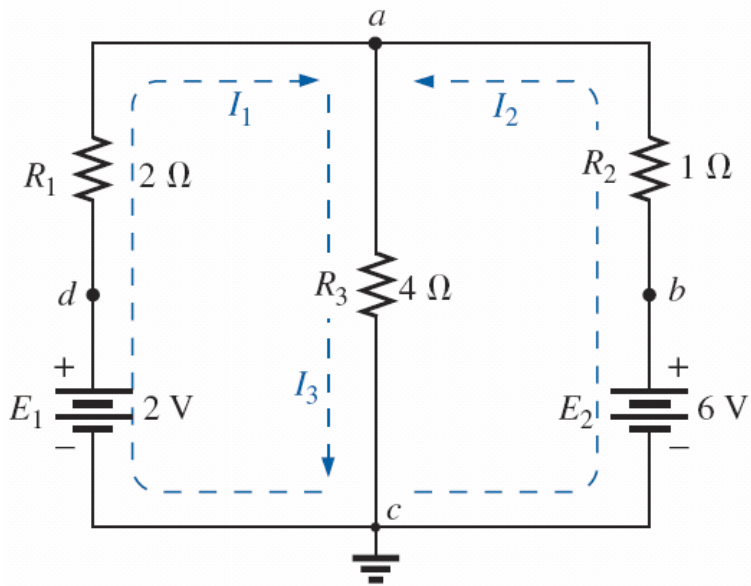
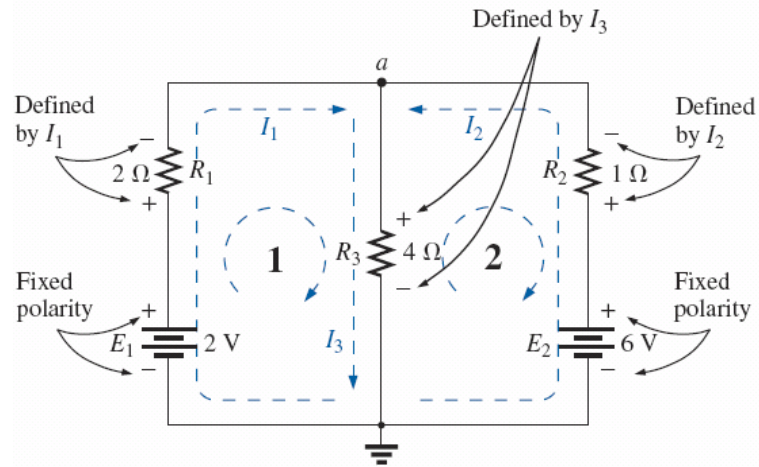Branch-Current Analysis Procedure

FIG. 8.22 *Example 8.9.*

FIG. 8.23 *Inserting the polarities across the resistive elements as defined by the chosen branch currents.*
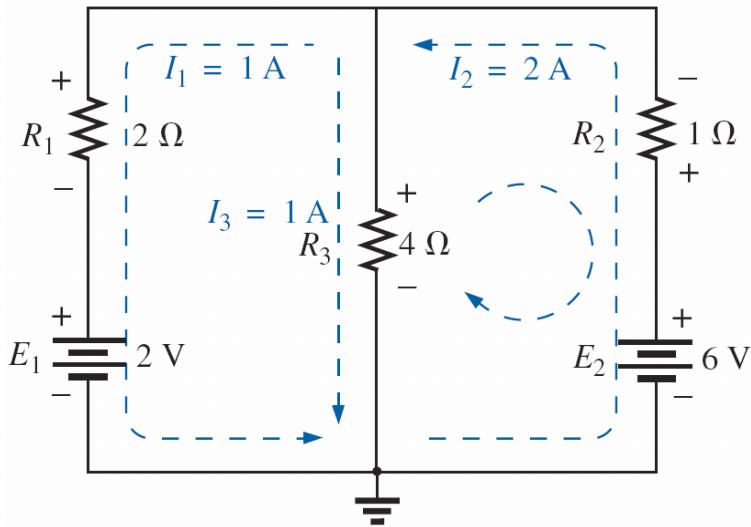
LOGO

Branch-Current Analysis Procedure

FIG. 8.25 *Reviewing the results of the analysis of the network in Fig. 8.22.*
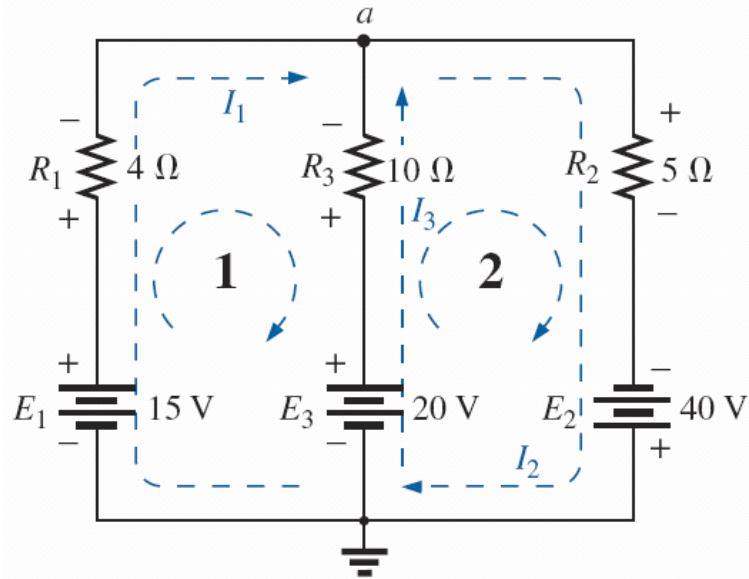
FIG. 8.26 *Example 8.10.*

LOGO

MESH ANALYSIS (GENERAL APPROACH)

❖ The next method to be described—**mesh analysis**—is actually an extension of the branch-current analysis approach just introduced.

❖ By defining a unique array of currents to the network, the information provided by the application of Kirchhoff's current law is already included when we apply Kirchhoff's voltage law. In other words, there is no need to apply step 4 of the branch-current method.

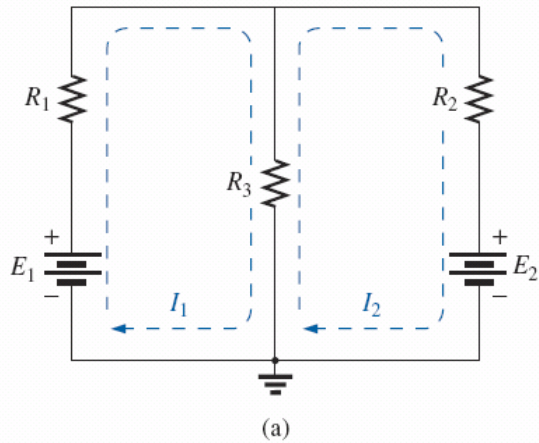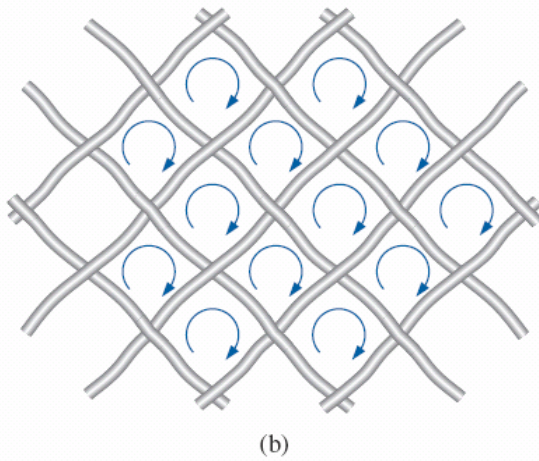❖ The currents to be defined are called **mesh** or **loop currents.**

FIG. 8.27 *Defining the mesh (loop) current: (a) "two-window" network; (b) wire mesh fence analogy.*

Mesh Analysis Procedure

1. *Assign a distinct current in the clockwise direction to each independent, closed loop of the network. It is not absolutely necessary to choose the clockwise direction for each loop current. In fact, any direction can be chosen for each loop current with no loss in accuracy, as long as the remaining steps are followed properly. However, by choosing the clockwise direction as a standard, we can develop a shorthand method (Section 8.8) for writing the required equations that will save time and possibly prevent some common errors.*

Mesh Analysis Procedure

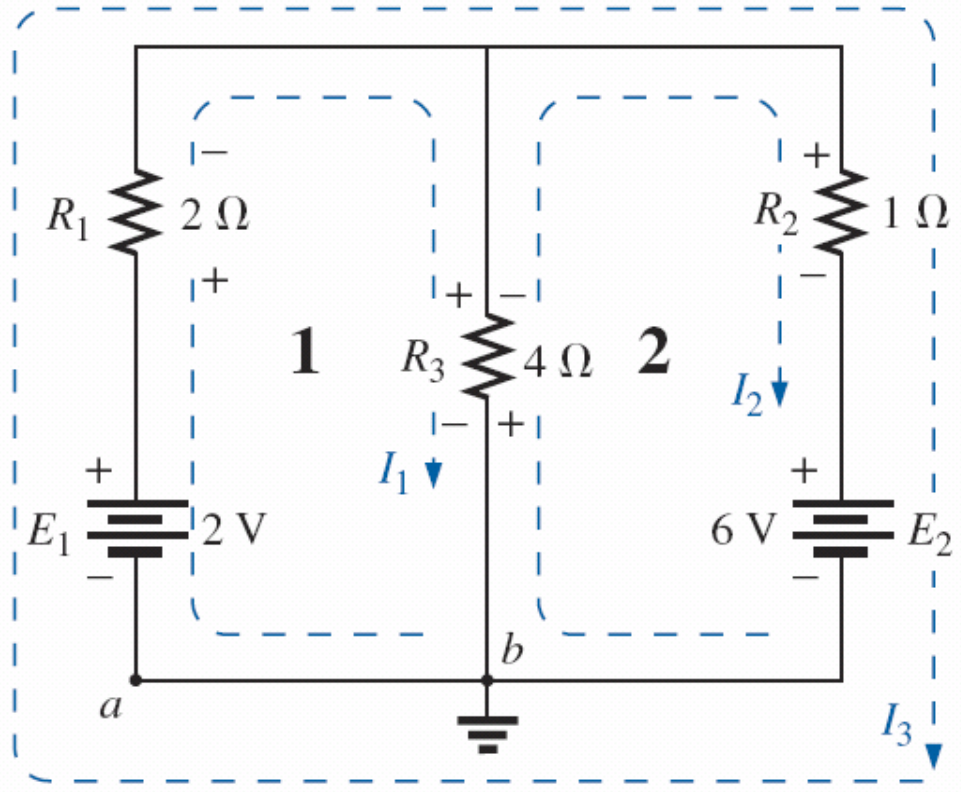**FIG. 8.28** *Defining the mesh currents for a "two-window" network.*

Mesh Analysis Procedure

2. *Indicate the polarities within each loop for each resistor as determined by the assumed direction of loop current for that loop. Note the requirement that the polarities be placed within each loop. This requires, as shown in Fig. 8.28, that the 4Ω resistor have two sets of polarities across it.*

3. *Apply Kirchhoff's voltage law around each closed loop in the clockwise direction. Again, the clockwise direction was chosen to establish uniformity and prepare us for the method to be introduced in the next section.*

- *a. If a resistor has two or more assumed currents through it, the total current through the resistor is the assumed current of the loop in which Kirchhoff's voltage law is being applied, plus the assumed currents of the other loops passing through in the same direction, minus the assumed currents through in the opposite direction.*

- *b. The polarity of a voltage source is unaffected by the direction of the assigned loop currents.*

Mesh Analysis Procedure

4. *Solve the resulting simultaneous linear equations for the assumed loop currents.*

Mesh Analysis Procedure
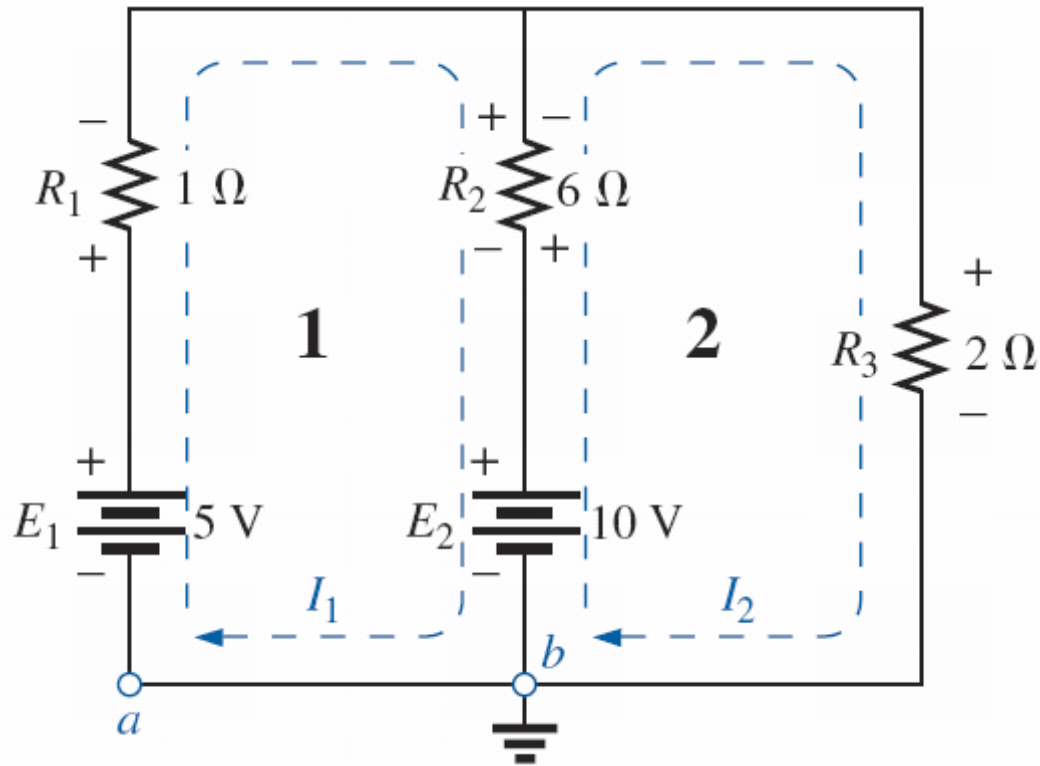
FIG. 8.29 *Example 8.12.*
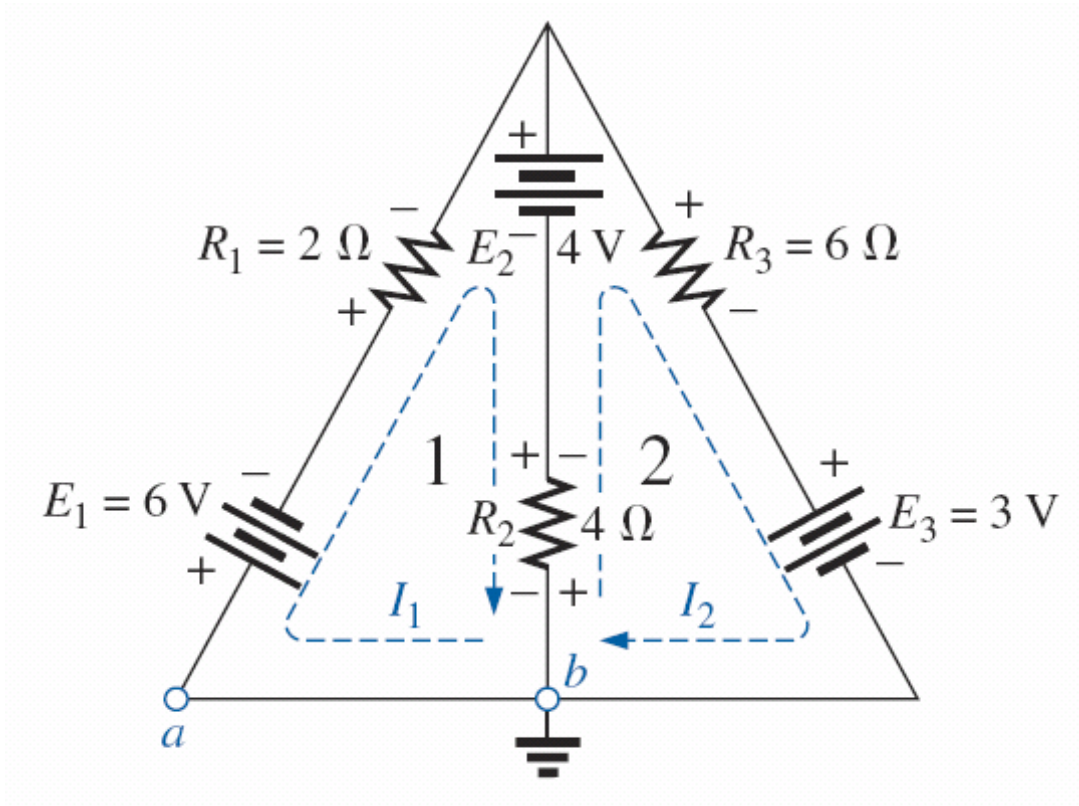
Mesh Analysis Procedure

FIG. 8.30 *Example 8.13.*

MESH ANALYSIS (GENERAL APPROACH)

Supermesh Currents

❖ Occasionally, you will find current sources in a network without a parallel resistance.

❖ This removes the possibility of converting the source to a voltage source as required by the given procedure.

Supermesh Currents

❖In such cases, you have a choice of two approaches.

- The simplest and most direct approach is to place a resistor in parallel with the current source that has a much higher value than the other resistors of the network.

- The other choice is to use the **supermesh approach.**

MESH ANALYSIS (GENERAL APPROACH)

Supermesh Currents
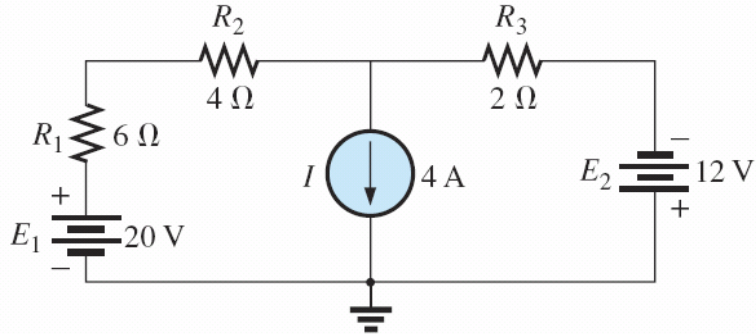
FIG. 8.31 *Example 8.14.*
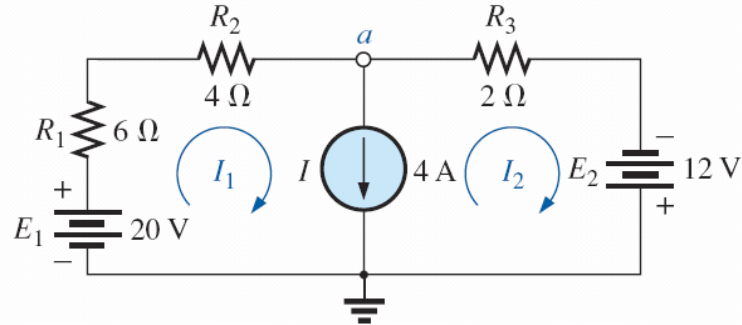
FIG. 8.32 *Defining the mesh currents for the network in Fig. 8.31.*

LOGO

Supermesh Currents
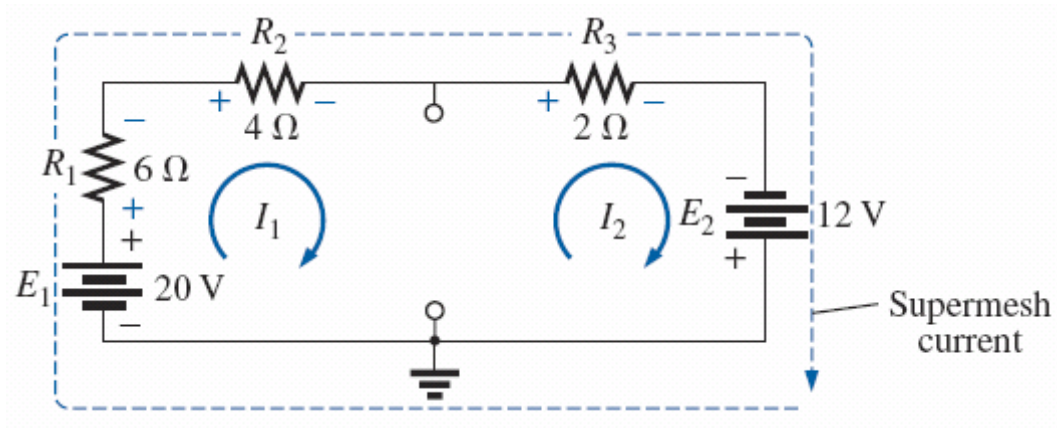
FIG. 8.33 *Defining the supermesh current.*

Supermesh Currents
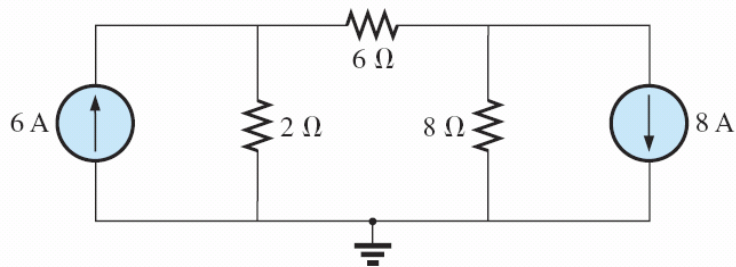
FIG. 8.34 *Example 8.15.*
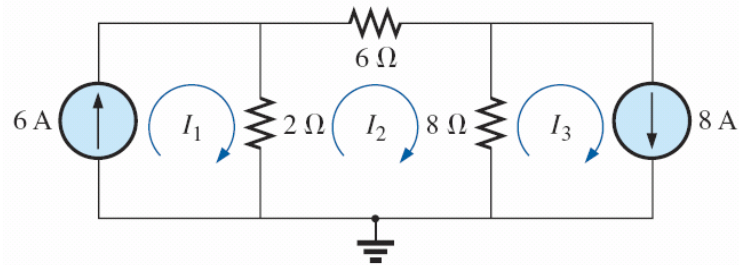
FIG. 8.35 *Defining the mesh currents for the network in Fig. 8.34.*

Supermesh Currents

FIG. 8.36 *Defining the supermesh current for the network in Fig. 8.34.*

MESH ANALYSIS (FORMAT APPROACH)

❖ As an aid in introducing the procedure, the network in Example 8.12 (Fig. 8.29) has been redrawn in Fig. 8.37 with the assigned loop currents.
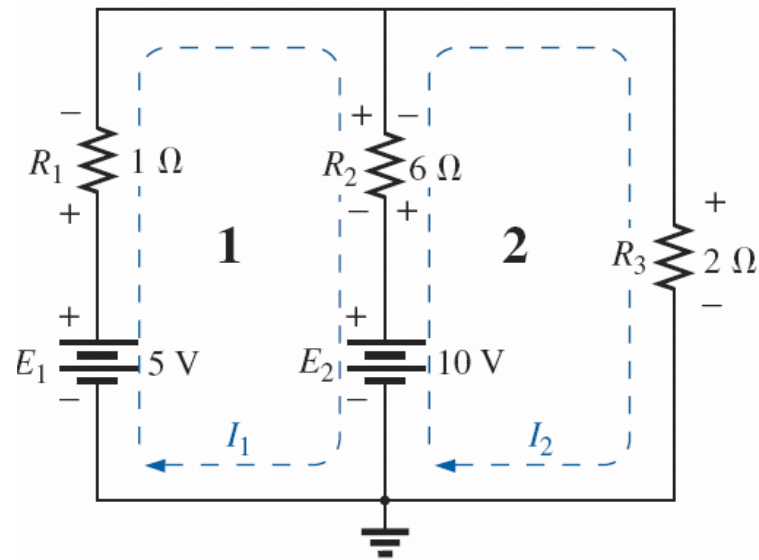
FIG. 8.37 *Network in Fig. 8.29 redrawn with assigned loop currents.*

MESH ANALYSIS (FORMAT APPROACH)

Mesh Analysis Procedure

1. *Assign a loop current to each independent, closed loop (as in the previous section) in a clockwise direction.*

2. *The number of required equations is equal to the number of chosen independent, closed loops. Column 1 of each equation is formed by summing the resistance values of those resistors through which the loop current of interest passes and multiplying the result by that loop current.*

Mesh Analysis Procedure

3. *We must now consider the mutual terms, which, as noted in the examples above, are always subtracted from the first column. A mutual term is simply any resistive element having an additional loop current passing through it. It is possible to have more than one mutual term if the loop current of interest has an element in common with more than one other loop current. This will be demonstrated in an example to follow. Each term is the product of the mutual resistor and the other loop current passing through the same element.*

Mesh Analysis Procedure

4. *The column to the right of the equality sign is the algebraic sum of the voltage sources through which the loop current of interest passes. Positive signs are assigned to those sources of voltage having a polarity such that the loop current passes from the negative to the positive terminal. A negative sign is assigned to those potentials for which the reverse is true.*

5. *Solve the resulting simultaneous equations for the desired loop currents.*

Mesh Analysis Procedure

FIG. 8.38 *Example 8.16.*

FIG. 8.39 *Example 8.17.*

LOGO

Mesh Analysis Procedure

FIG. 8.40 *Example 8.18.*

Mesh Analysis Procedure

$$\frac{\det\begin{bmatrix} 11 & -3 & 15 \\ -3 & 10 & 0 \\ -8 & -5 & 0 \end{bmatrix}}{\det\begin{bmatrix} 11 & -3 & -8 \\ -3 & 10 & -5 \\ -8 & -5 & 23 \end{bmatrix}} \qquad \mathbf{1.22E0}$$

FIG. 8.42 *The resulting display after properly entering the data for the current I_3.*

NODAL ANALYSIS (GENERAL APPROACH)

❖ The methods introduced thus far have all been to find the currents of the network

❖ We now turn our attention to **nodal analysis**—a method that provides the nodal voltages of a network, that is, the voltage from the various **nodes** (junction points) of the network to ground.

❖ The method is developed through the use of Kirchhoff's current law in much the same manner as Kirchhoff's voltage law was used to develop the mesh analysis approach.

NODAL ANALYSIS (GENERAL APPROACH)

❖ *The number of nodes for which the voltage must be determined using nodal analysis is 1 less than the total number of nodes.*

❖ *The number of equations required to solve for all the nodal voltages of a network is 1 less than the total number of independent nodes.*

Nodal Analysis Procedure

1. *Determine the number of nodes within the network.*

2. *Pick a reference node, and label each remaining node with a subscripted value of voltage: V1, V2, and so on.*

Nodal Analysis Procedure

3. *Apply Kirchhoff's current law at each node except the reference. Assume that all unknown currents leave the node for each application of Kirchhoff's current law. In other words, for each node, don't be influenced by the direction that an unknown current for another node may have had. Each node is to be treated as a separate entity, independent of the application of Kirchhoff's current law to the other nodes.*

4. *Solve the resulting equations for the nodal voltages.*

Nodal Analysis Procedure

FIG. 8.43 *Example 8.19.*
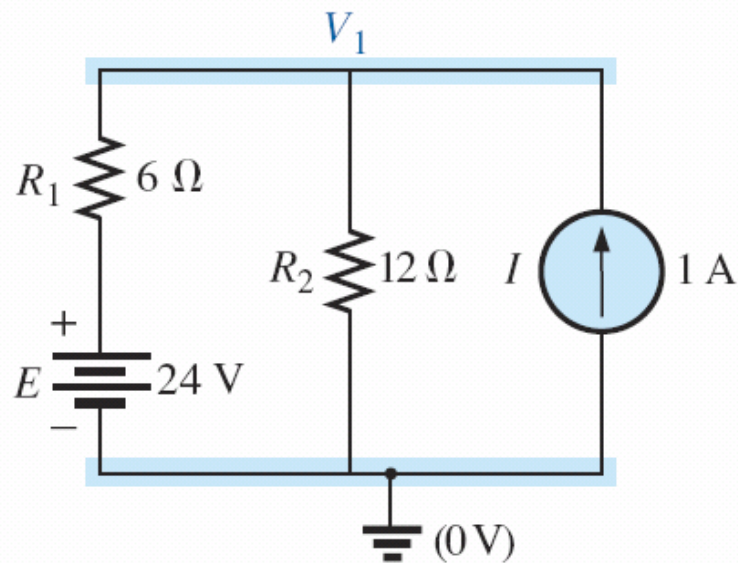
FIG. 8.44 *Network in Fig. 8.43 with assigned nodes.*

Nodal Analysis Procedure

FIG. 8.45 *Applying Kirchhoff 's current law to the node V_1.*
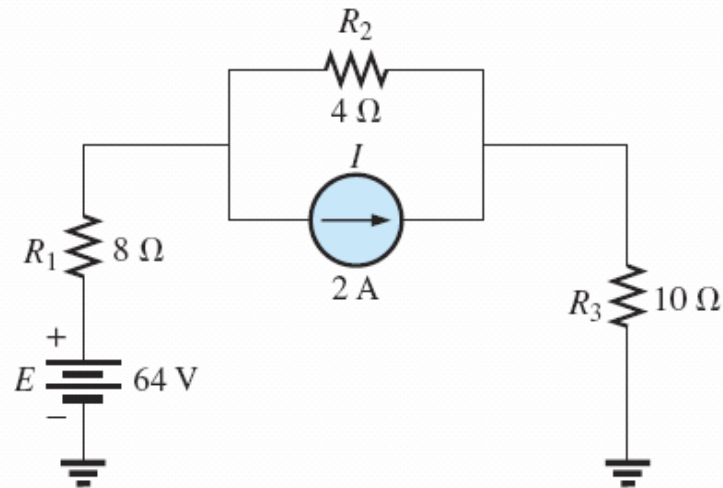
FIG. 8.46 *Example 8.20.*

Nodal Analysis Procedure

FIG. 8.47 *Defining the nodes for the network in Fig. 8.46.*
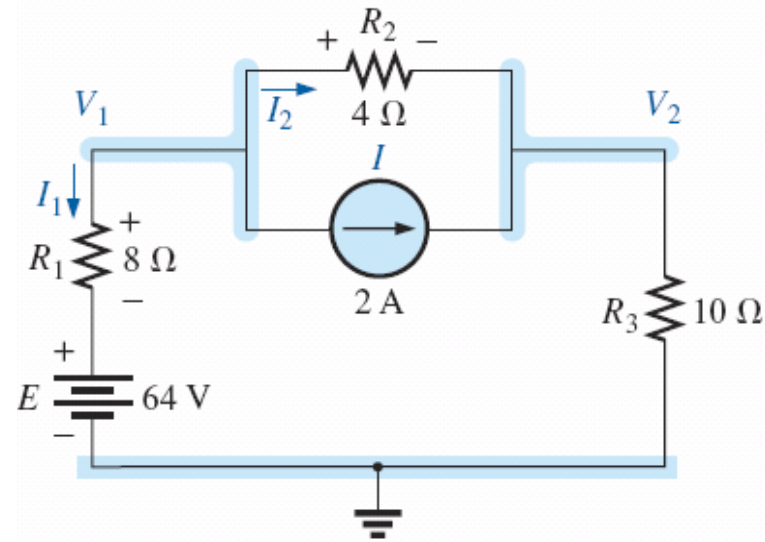
FIG. 8.48 *Applying Kirchhoff 's current law to node V1.*

LOGO

Nodal Analysis Procedure

FIG. 8.49 *Applying Kirchhoff's current law to node V_2.*

Nodal Analysis Procedure

FIG. 8.50 *Example 8.21.*
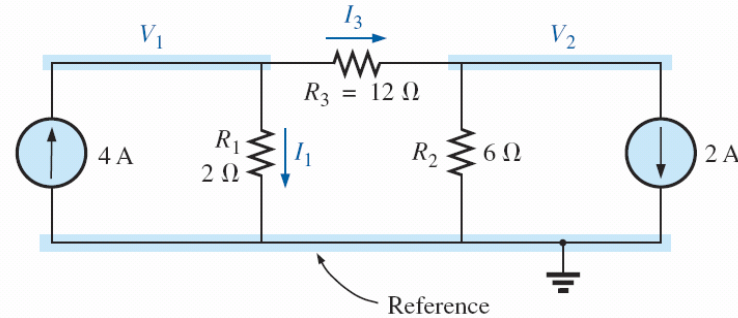
FIG. 8.51 *Defining the nodes and applying Kirchhoff 's current law to the node V_1.*

LOGO

Nodal Analysis Procedure

FIG. 8.52 *Applying Kirchhoff's current law to the node V_2.*

Supernode

❖ Occasionally, you may encounter voltage sources in a network that do not have a series internal resistance that would permit a conversion to a current source.

❖ In such cases, you have two options.

- The simplest and most direct approach is to *place a resistor in series with the source of a very small value compared to the other resistive elements of the network.*

- The other approach is to use the **supernode approach**
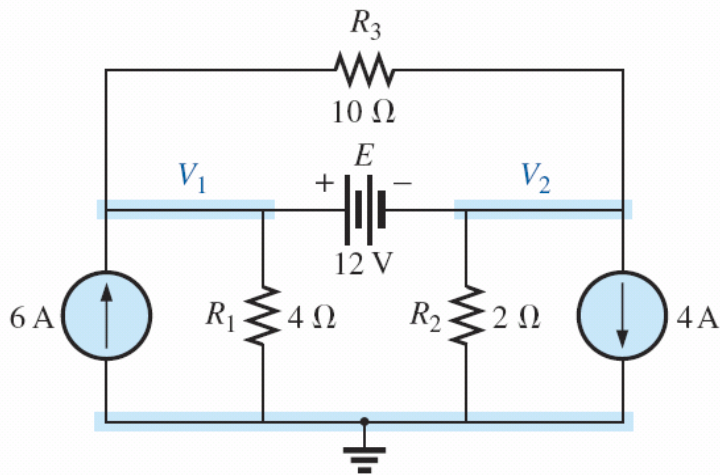
Supernode

FIG. 8.53 *Example 8.22.*
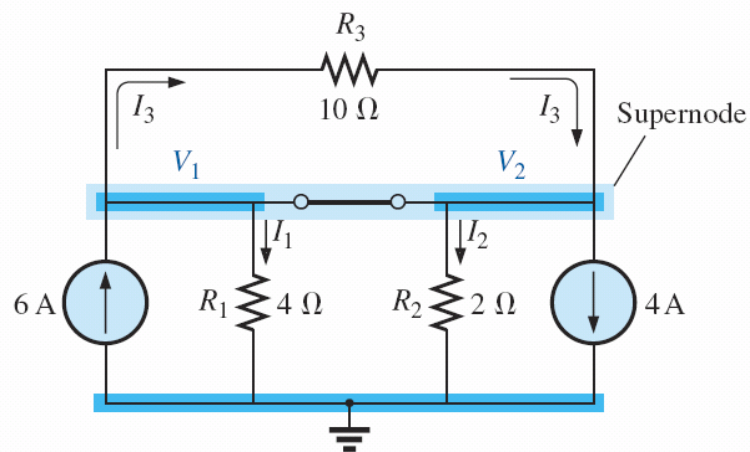
FIG. 8.54 *Defining the supernode for the network in Fig. 8.53.*

Nodal Analysis Procedure

1. *Choose a reference node, and assign a subscripted voltage label to the (N - 1) remaining nodes of the network.*

2. *The number of equations required for a complete solution is equal to the number of subscripted voltages (N - 1). Column 1 of each equation is formed by summing the conductances tied to the node of interest and multiplying the result by that subscripted nodal voltage.*

Nodal Analysis Procedure

3. *We must now consider the mutual terms, which, as noted in the preceding example, are always subtracted from the first column. It is possible to have more than one mutual term if the nodal voltage of current interest has an element in common with more than one other nodal voltage. This is demonstrated in an example to follow. Each mutual term is the product of the mutual conductance and the other nodal voltage, tied to that conductance.*

Nodal Analysis Procedure

4.   *The column to the right of the equality sign is the algebraic sum of the current sources tied to the node of interest. A current source is assigned a positive sign if it supplies current to a node and a negative sign if it draws current from the node.*

5.   *Solve the resulting simultaneous equations for the desired voltages.*

Nodal Analysis Procedure
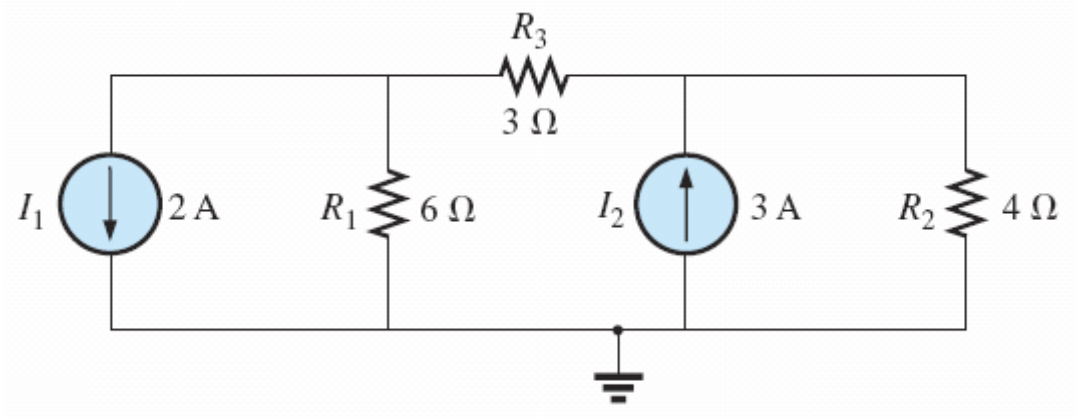
FIG. 8.55 *Example 8.23.*

Nodal Analysis Procedure
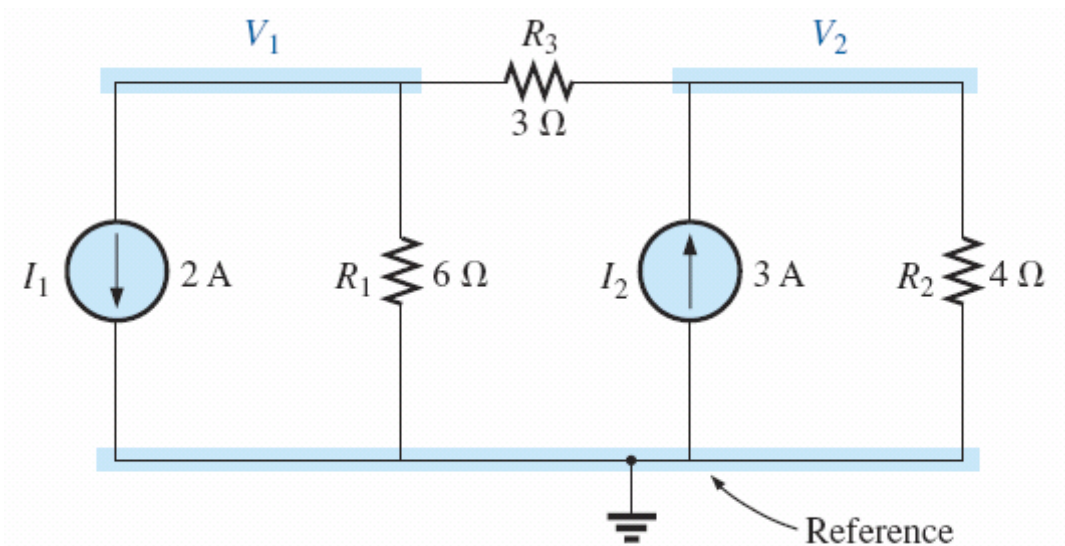
FIG. 8.56 *Defining the nodes for the network in Fig. 8.55.*

Nodal Analysis Procedure
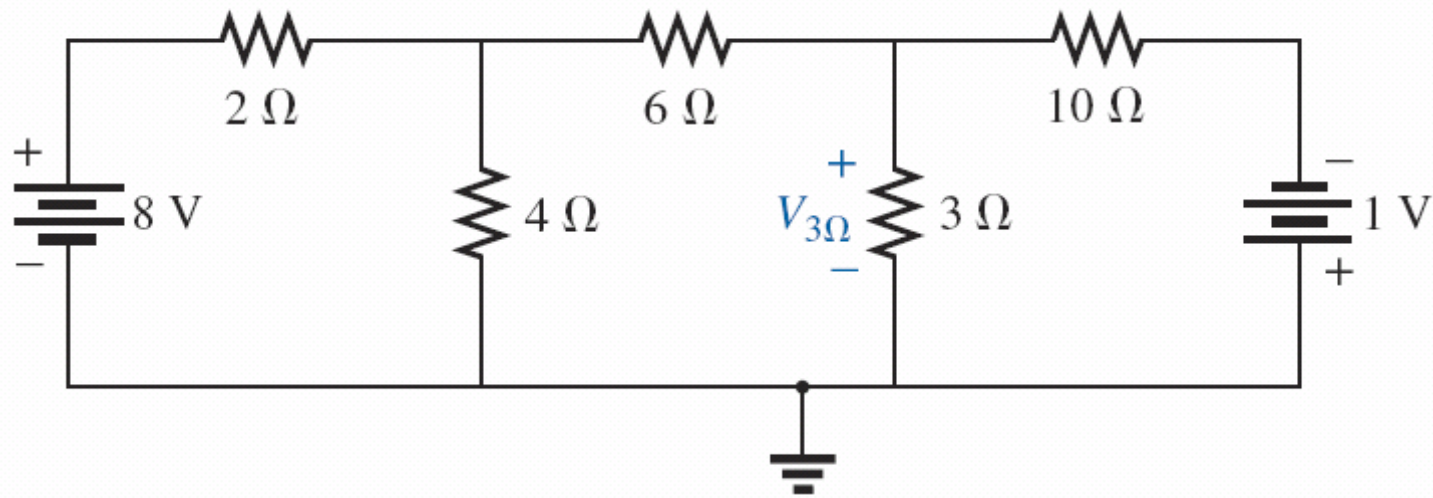
FIG. 8.57 *Example 8.24.*

Nodal Analysis Procedure
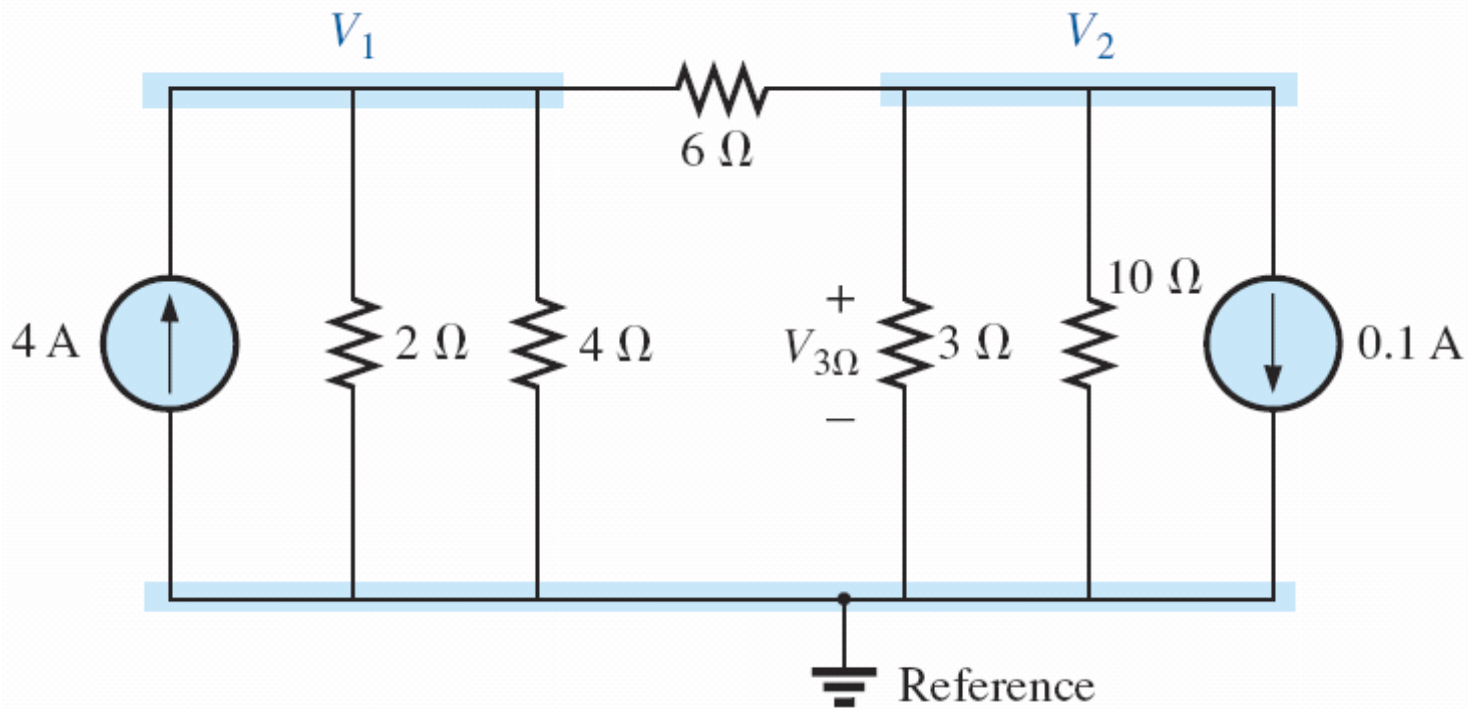
FIG. 8.58 *Defining the nodes for the network in Fig. 8.57.*

Nodal Analysis Procedure
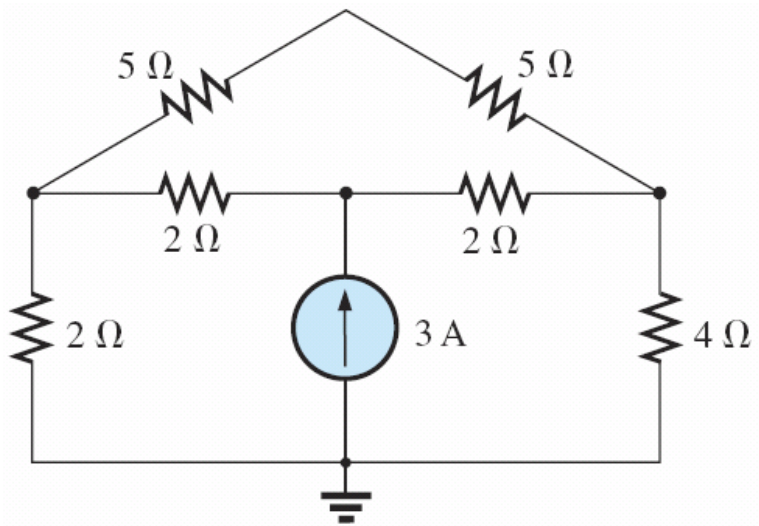
FIG. 8.59 *Example 8.25.*
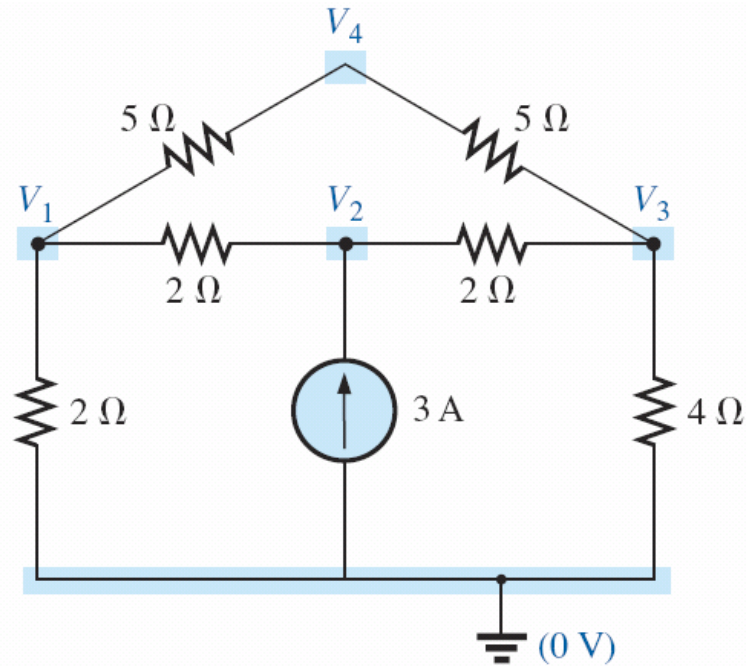
FIG. 8.60 *Defining the nodes for the network in Fig. 8.59.*

Nodal Analysis Procedure
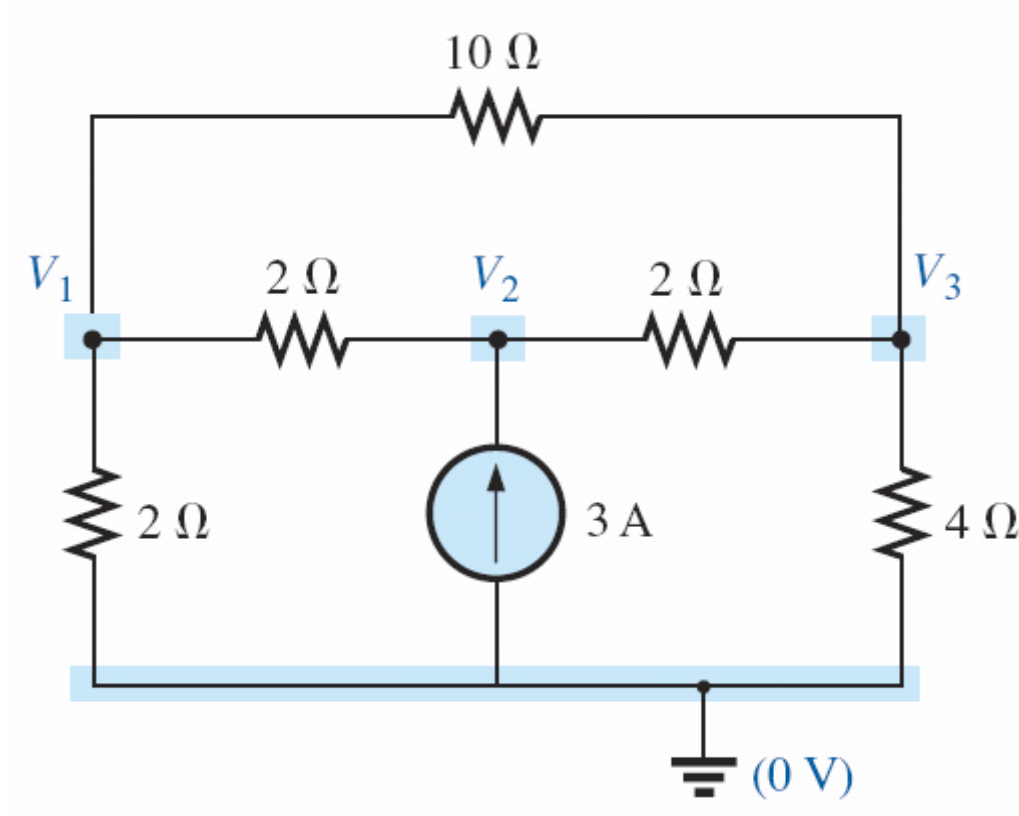
FIG. 8.61 *Reducing the number of nodes for the network in Fig. 8.59 by combining the two 5Ω resistors.*

Nodal Analysis Procedure
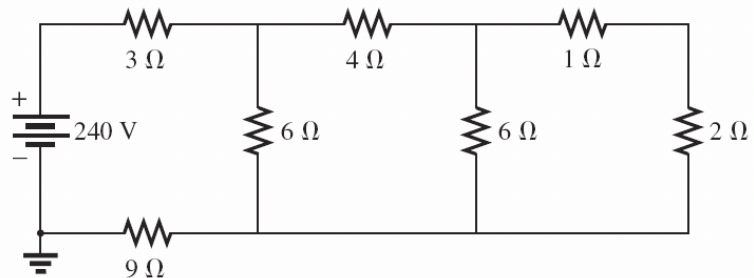
FIG. 8.62 *Example 8.26.*
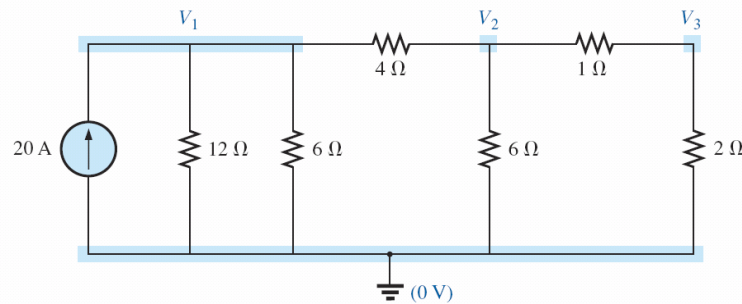
FIG. 8.63 *Converting the voltage source to a current source and defining the nodes for the network in Fig. 8.62.*
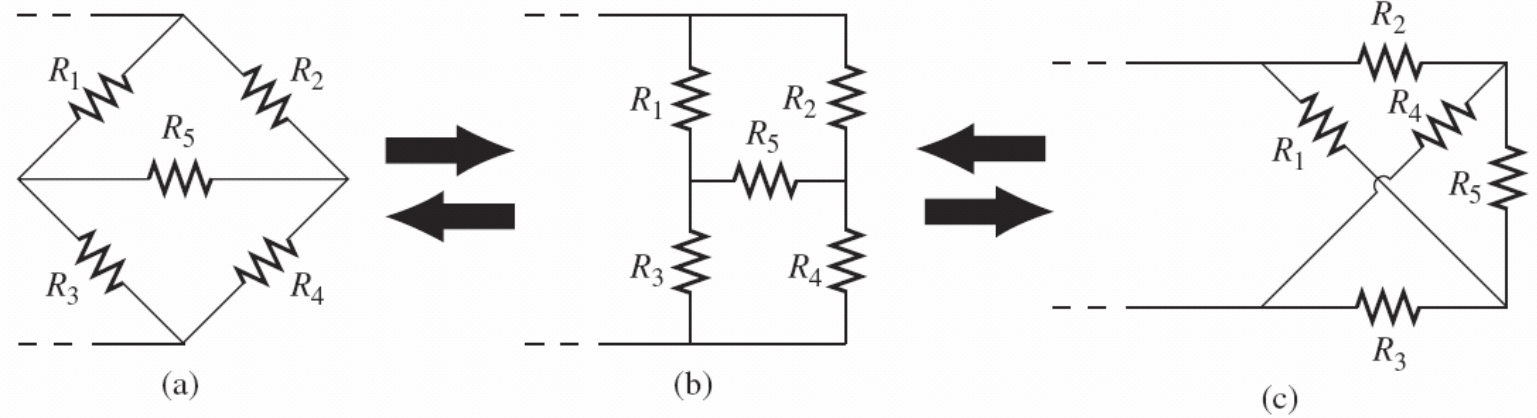
FIG. 8.64 *Various formats for a bridge network.*

BRIDGE NETWORKS
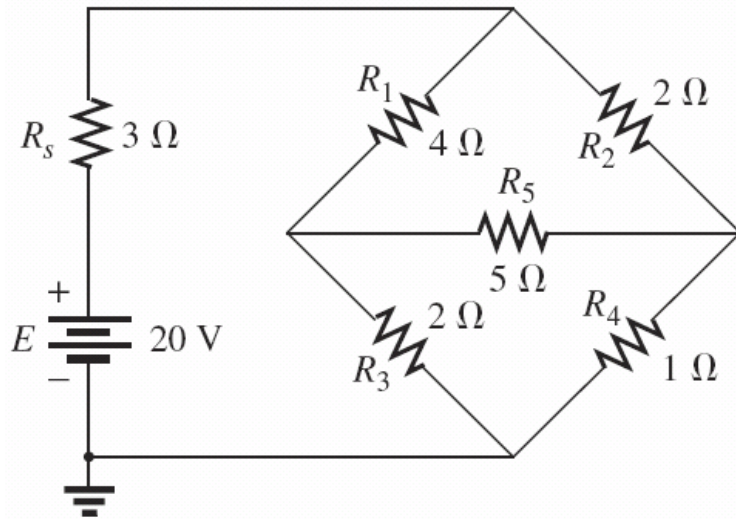
FIG. 8.65 *Standard bridge configuration.*
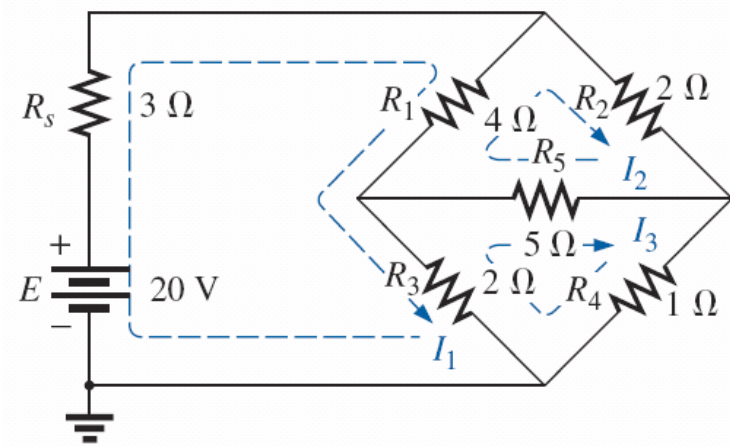
FIG. 8.66 *Assigning the mesh currents to the network in Fig. 8.65.*

BRIDGE NETWORKS
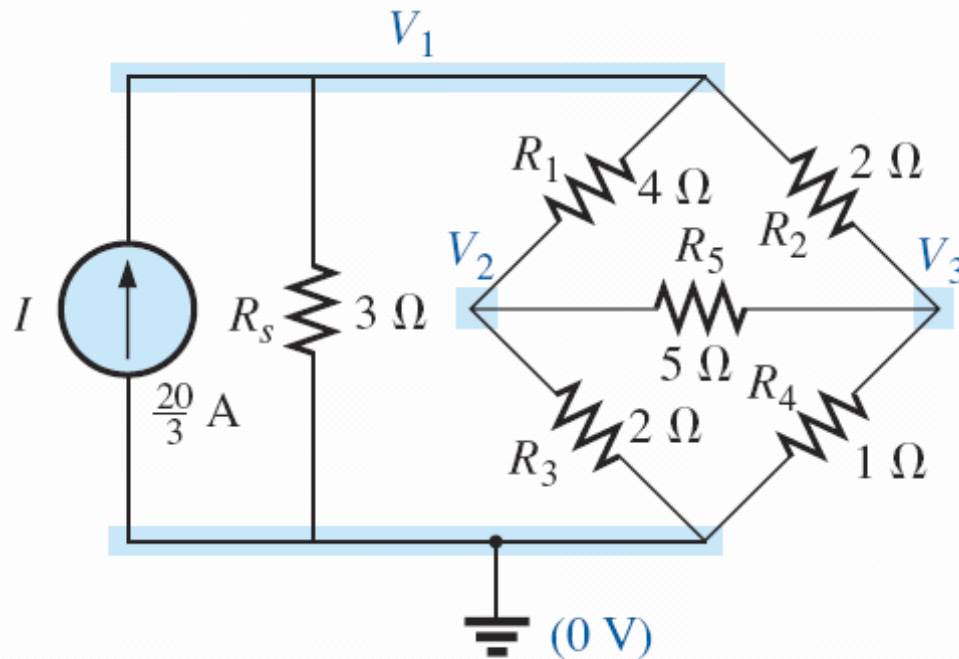
FIG. 8.67 *Defining the nodal voltages for the network in Fig. 8.65.*

FIG. 8.71 *Substituting the short-circuit equivalent for the balance arm of a balanced bridge.*
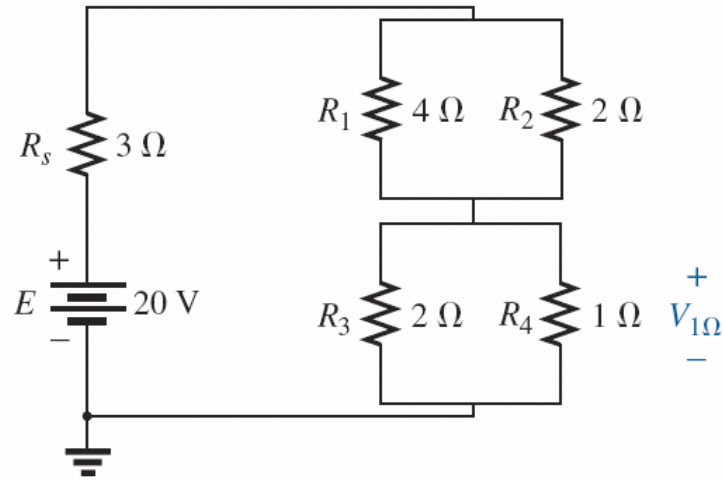
FIG. 8.72 *Redrawing the network in Fig. 8.71.*

LOGO

FIG. 8.73 *Substituting the open-circuit equivalent for the balance arm of a balanced bridge.*

TI-89 Calculator Solution
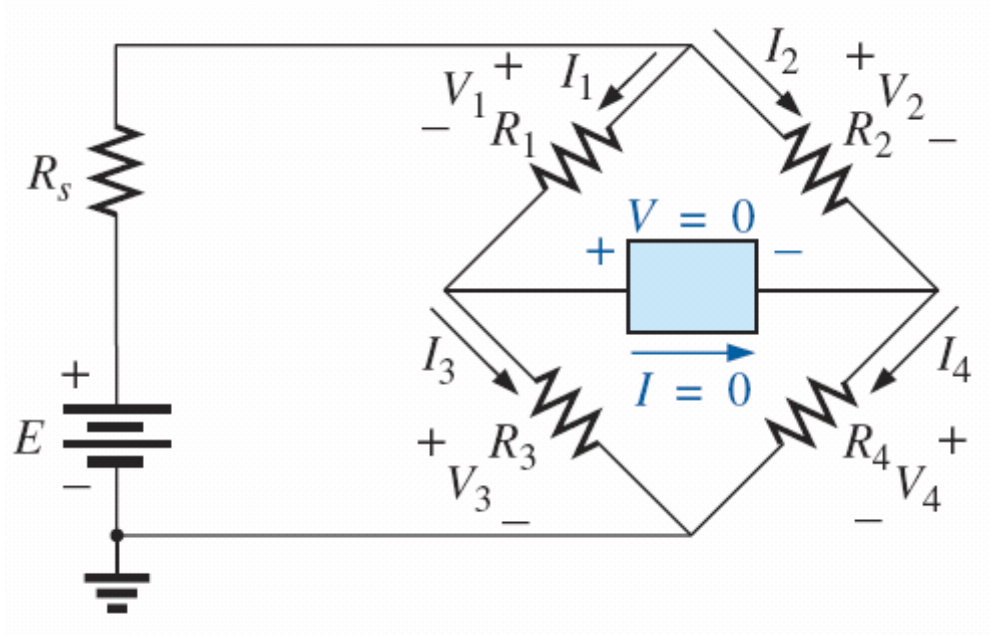
FIG. 8.74 *Establishing the balance criteria for a bridge network.*
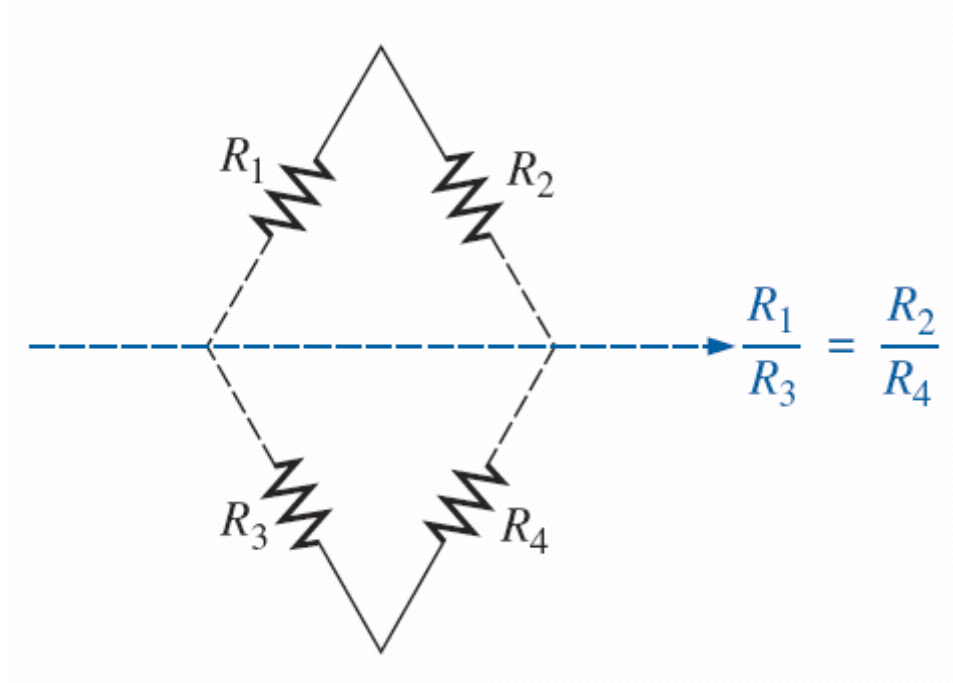
FIG. 8.75 *A visual approach to remembering the balance condition.*

$$\frac{R_1}{R_3} = \frac{R_2}{R_4}$$

Y-Δ (T-π) AND Δ-Y (π-T) CONVERSIONS

❖ Circuit configurations are often encountered in which the resistors do not appear to be in series or parallel.

❖ Under these conditions, it may be necessary to convert the circuit from one form to another to solve for any unknown quantities if mesh or nodal analysis is not applied.

❖ Two circuit configurations that often account for these difficulties are the **wye (Y)** and **delta (Δ) configurations** depicted in Fig. 8.76(a).

❖ They are also referred to as the **tee (T)** and **pi (π),** respectively,
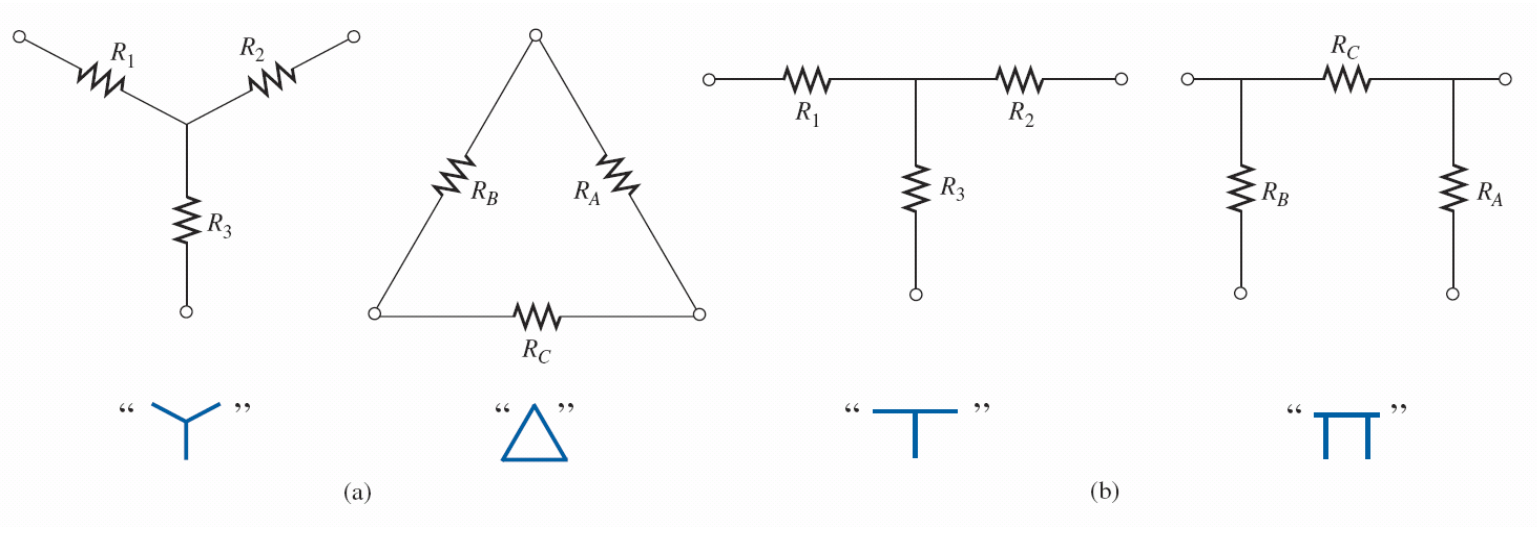
FIG. 8.76 *The Y (T) and Δ (π) configurations.*
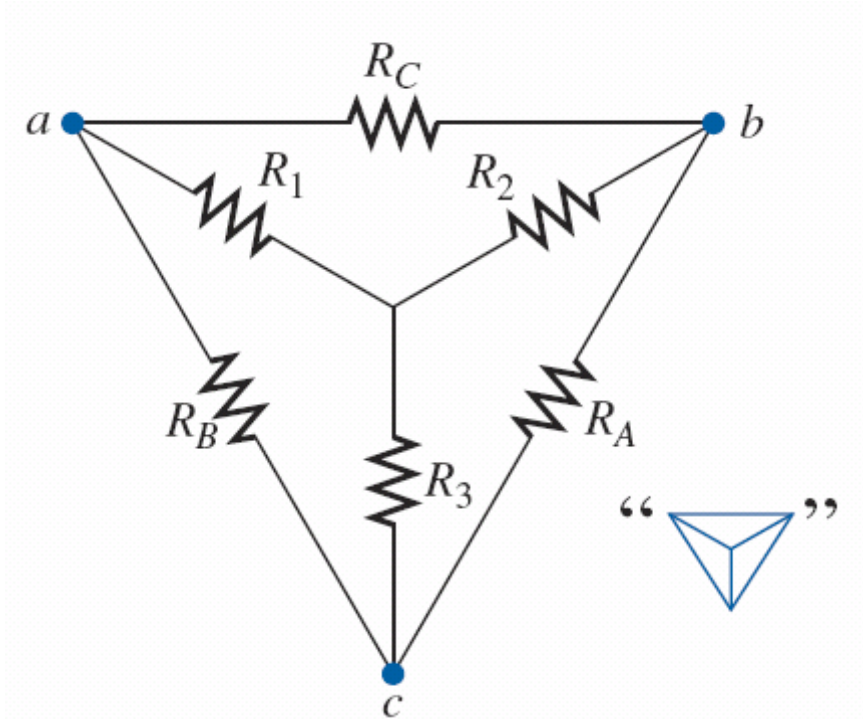
FIG. 8.77 *Introducing the concept of Δ-Y or Y-Δ conversions*
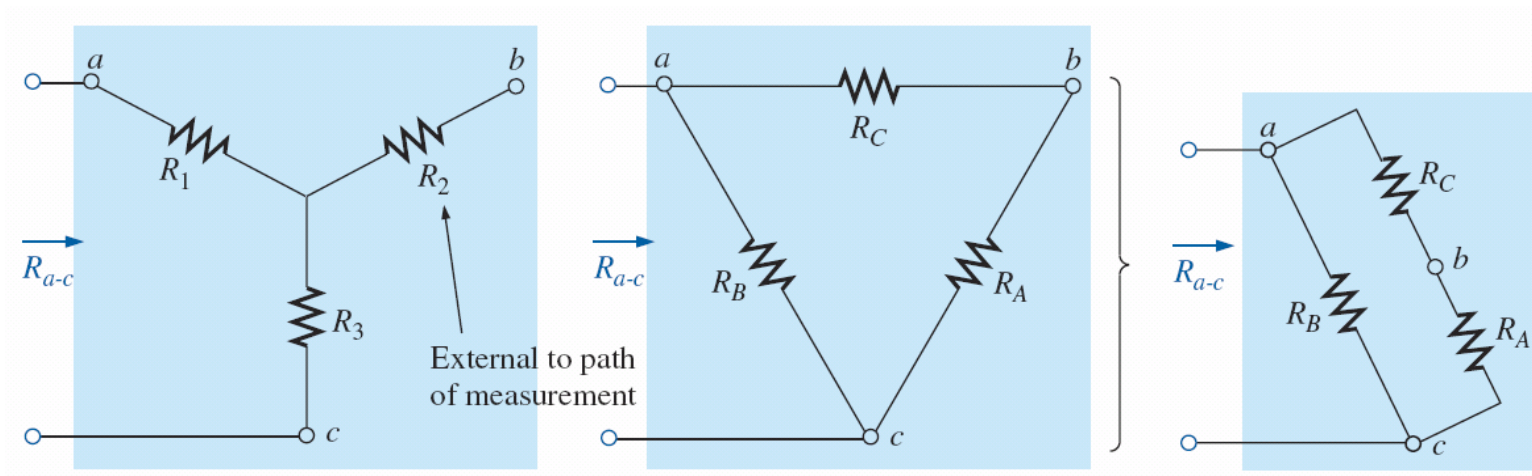
FIG. 8.78 *Finding the resistance $R_{a\text{-}c}$ for the Y and Δ configurations.*
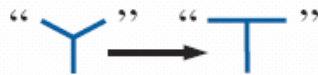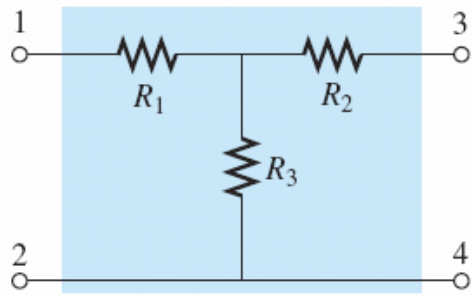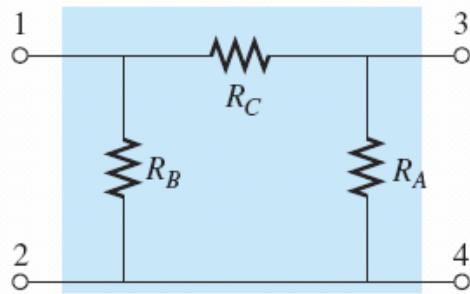
FIG. 8.79 *The relationship between the Y and T configurations and the Δ and π configurations.*
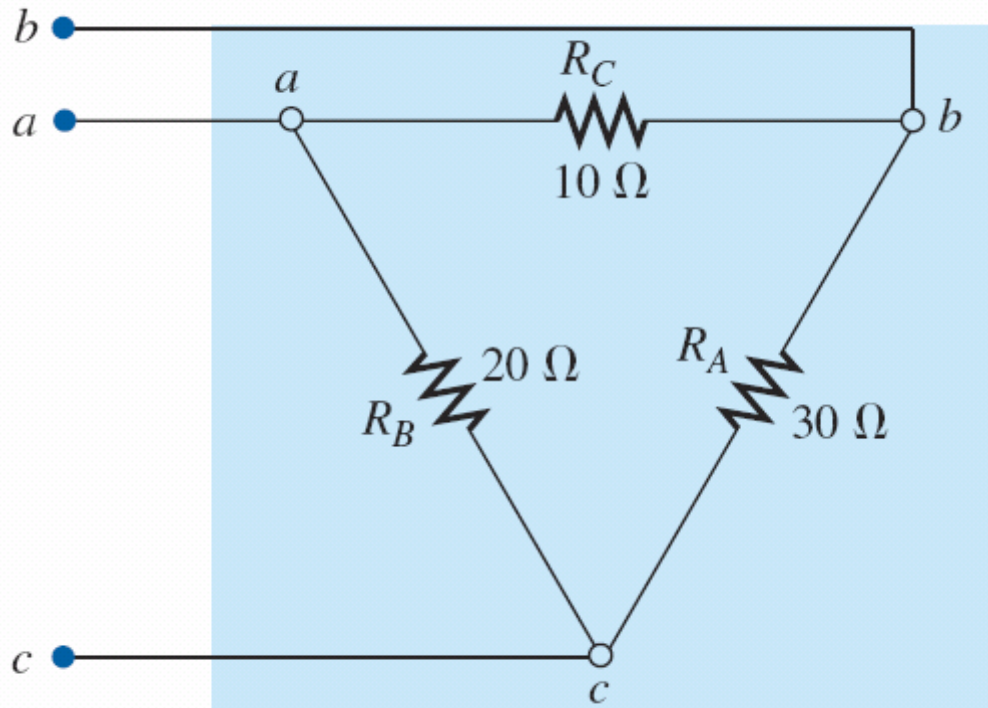
Y-Δ (T-π) AND Δ-Y (π-T) CONVERSIONS

FIG. 8.80 *Example 8.27.*
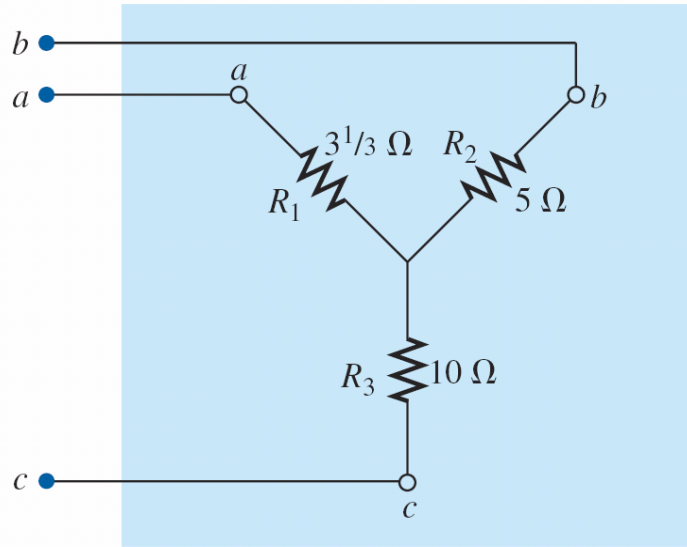
FIG. 8.81 *The Y equivalent for the Δ in Fig. 8.80.*
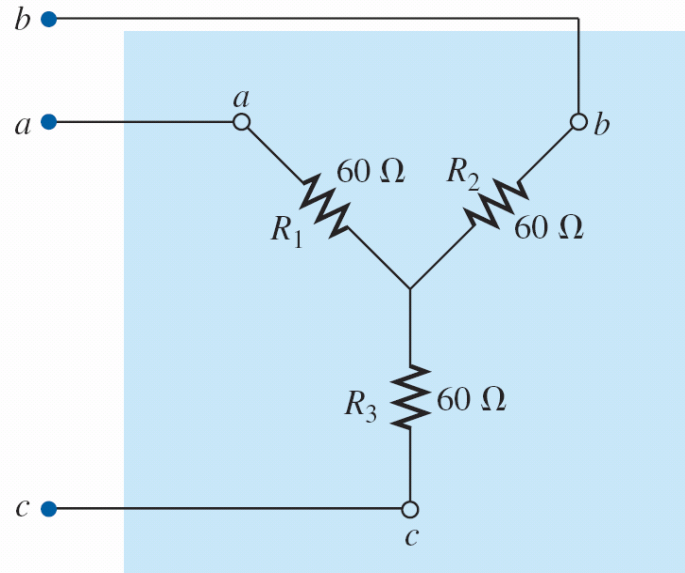
FIG. 8.82 *Example 8.28.*
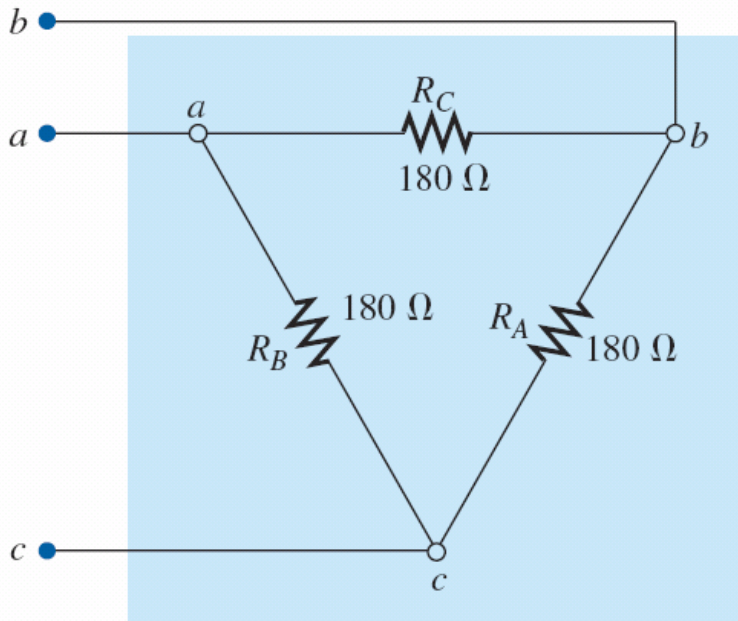
FIG. 8.83 *The Δ equivalent for the Y in Fig. 8.82.*
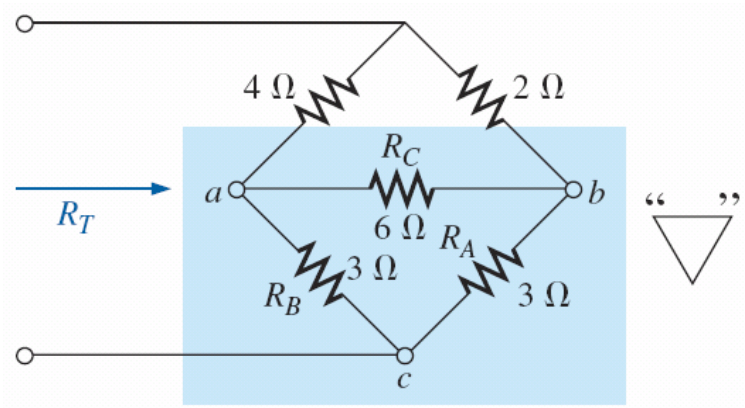
FIG. 8.84 *Example 8.29.*
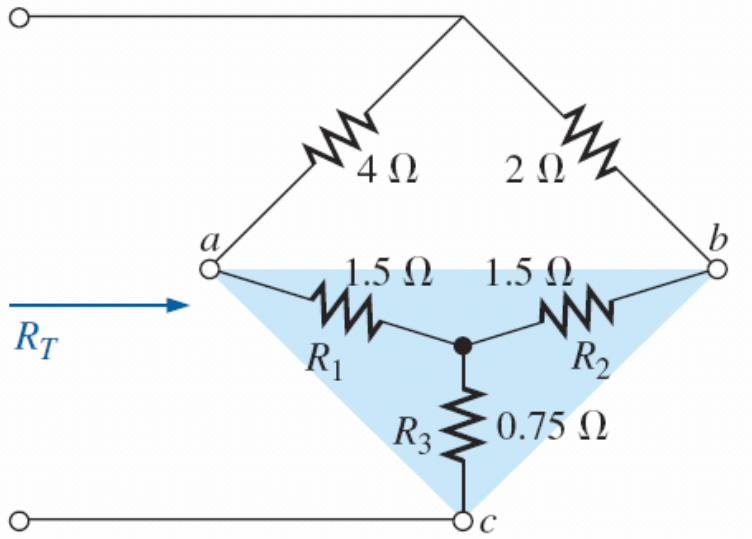
FIG. 8.85 *Substituting the Y equivalent for the bottom Δ in Fig. 8.84.*
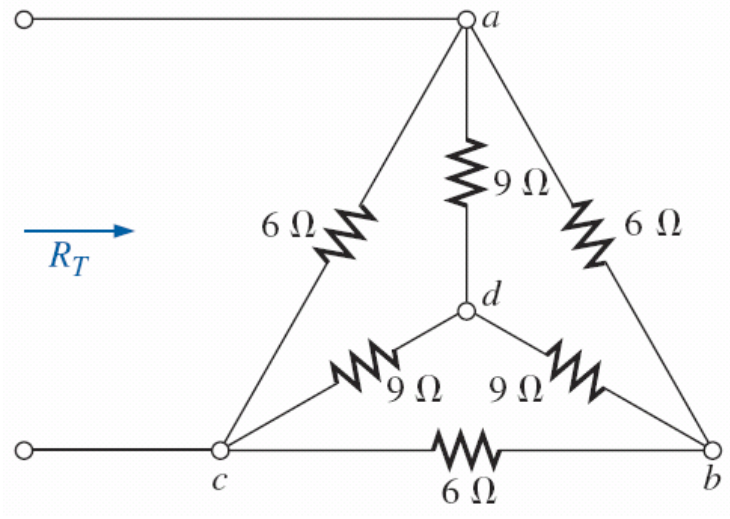
FIG. 8.86 *Example 8.30.*
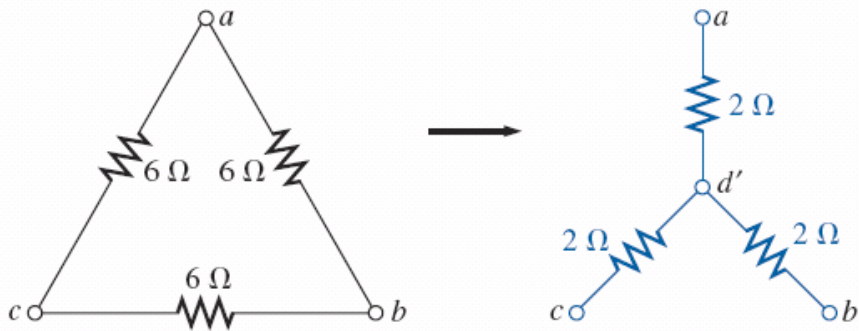
FIG. 8.87 *Converting the Δ configuration of Fig. 8.86 to a Y configuration.*
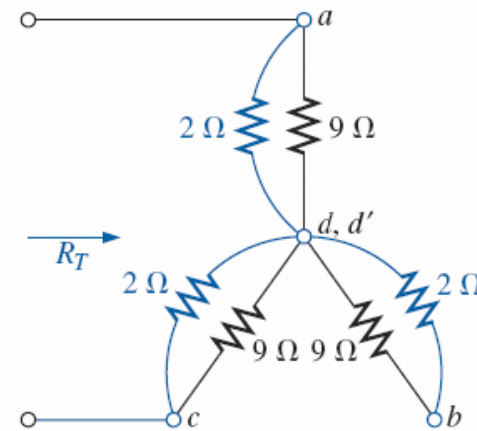
FIG. 8.88 *Substituting the Y configuration for the converted Δ into the network in Fig. 8.86.*
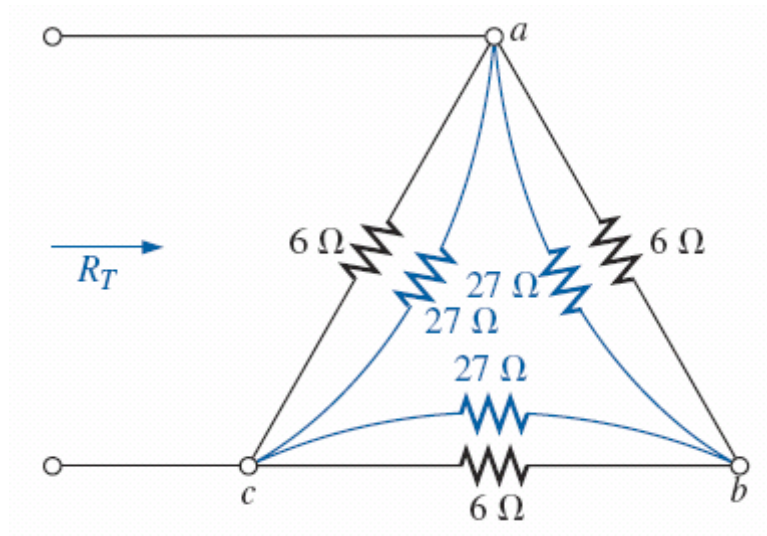
FIG. 8.89 *Substituting the converted Y configuration into the network in Fig. 8.86.*

COMPUTER ANALYSIS
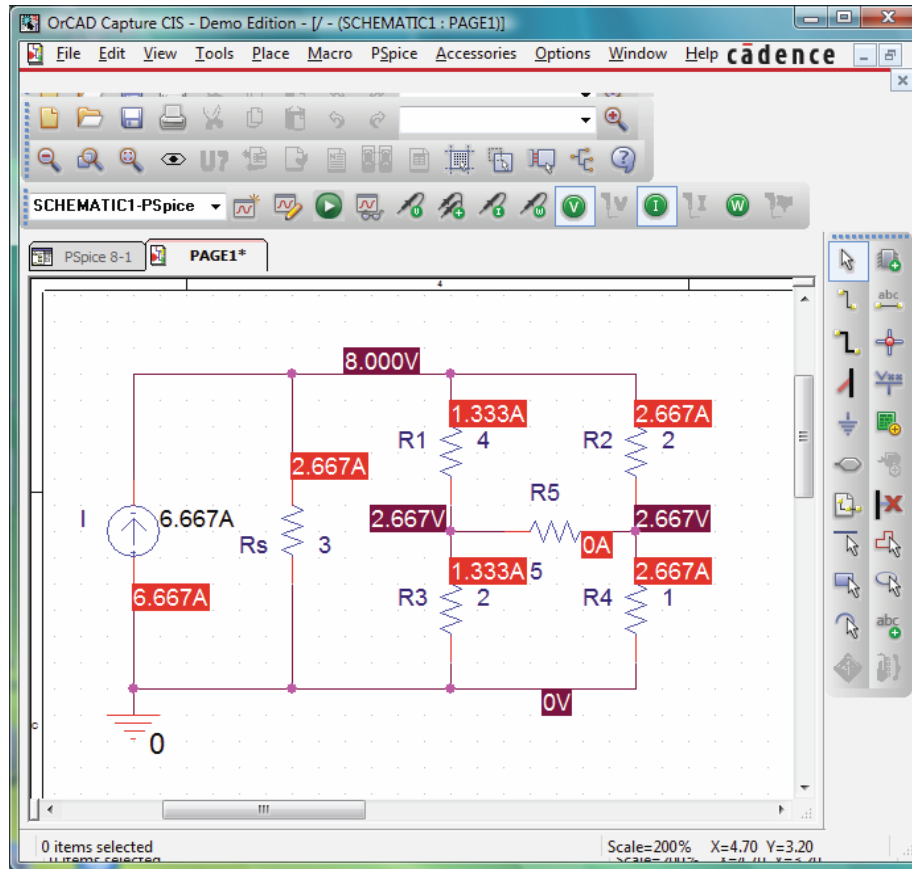
PSpice

FIG. 8.95 *Applying PSpice to the bridge network in Fig. 8.67.*
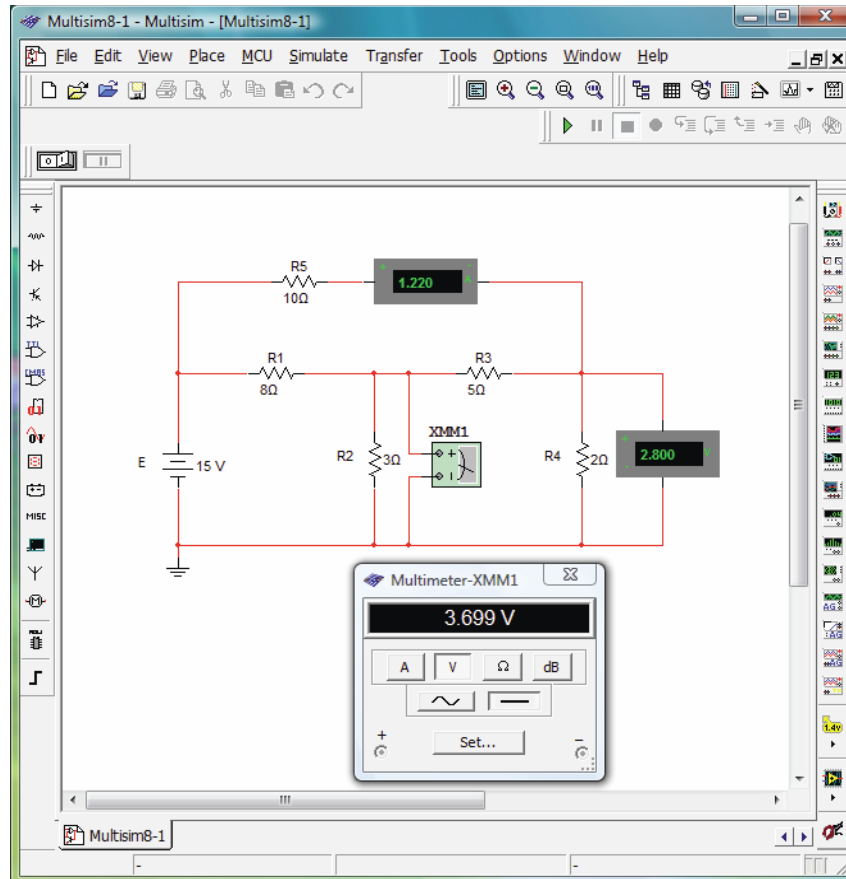
COMPUTER ANALYSIS

Multisim

FIG. 8.96 *Using Multisim to verify the results in Example 8.18.*

Thank You !